coolteq.h Modulator

USER GUIDE **AN002098**

1 Introduction

This application note gives guidelines on how to implement a digital envelope tracking amplifier system using the Nujira coolteq.h™ Modulator, focusing on system architecture, baseband and DPD considerations as well as coolteq.h™ Modulator control. It assumes that the reader is already familiar with digital amplifier design principles and the NCT-H4010/ NCT-H3009 datasheets. For aspects such as RF, mechanical and layout design please refer to the coolteq.h™ Modulator Design Guide [1].

2 HAT Overview

The coolteq.h™ Modulator enables design of ultra high efficiency high crest factor RF power amplifiers with support for a wide range of PAPRs. The coolteq.h™ Modulator design is RF frequency agnostic and operates in 20MHz RF Bandwidth. Time Division Duplex (TDD) mode for WCDMA and WiMAX technologies is supported with in-band TDD signal through drain envelope LVDS input or a dedicated TDD signal input.

2.1 coolteq.h™ Modulator Interfaces

The inputs and output interfaces of the coolteq.h™ Modulator are shown in **Figure 1**.

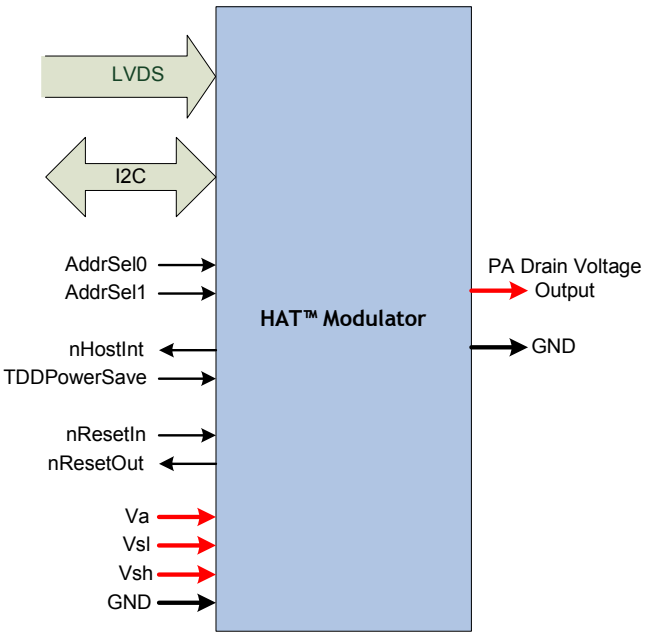

Figure 1. coolteq.h™ Modulator Interfaces

The coolteq.h™ Modulator interfaces are:

- LVDS Envelope Reference Data Interface: 14 bit drain envelope reference and associated clock input
- Control & Monitor Interface: Bidirectional I^2C slave
- I^2C address selection inputs: four slave addresses
- nHostInt output for Alarm and Warning interrupts to Host (Baseband Controller)
- TDDPowerSave input for TDD Mode Power Save signalling
- nResetIn and nResetOut for coolteq.h™ Modulator external reset input and outputs respectively
- Vsl, Vsh Main and Va Auxiliary supply inputs
- PA Drain Voltage Modulated Output: output to RF device drain

For the physical locations and pin assignment information of these interfaces please refer to [2]. The following sections give more information on each of these interfaces.

2.1.1 LVDS Envelope Reference Data Interface

The LVDS Envelope Reference Data Interface consists of 14 bit parallel data at a nominal rate of **122.88MSPS** and associated clock signal at **122.88MHz**. The coolteq.h™ Modulator is able to tolerate a limited range of sampling rates around this nominal value, for exact specifications please refer to [2].

The required PA Drain Voltage Output is linearly encoded on the LVDS Envelope Reference Data interface, '0' corresponding to the minimum output voltage and 2^{14}-1 corresponding to the maximum output voltage.

The data sampling point relative to the clock phase can be adjusted via the Control & Monitor Interface [3].

The LVDS Envelope Reference Data Interface lines are terminated internally to the coolteq.h™ Modulator.

2.1.2 Power Supplies

coolteq.h™ Modulator has three power supply inputs (Va) Auxiliary and (Vsl, Vsh) Main power supplies. These supply line can be switched on and off without any sequence restriction.

2.1.3 Control & Monitor Interface

The Control & Monitor Interface is used to manage the coolteq.h™ Modulator through register reads and writes. It utilises a standard I^2C physical interface and is compliant with the I^2C Fast mode of Version 2.1 of the I^2C Bus Specification [4]. It implements 7-bit addressing and clock stretching. The main functions of Control & Monitor Interface are:

- coolteq.h™ Modulator PA Drain Voltage Modulation start and stop
- Report coolteq.h™ Modulator status – temperature, warning & alarm states
- Reset coolteq.h™ Modulator warning & alarm states
- Report coolteq.h™ Modulator product serial numbers
- Configure coolteq.h™ Modulator parameters
- Enable/Disable coolteq.h™ Modulator functions
- Switching between coolteq.h™ Modulator Configuration Sets
- SW/FW download

For more information on the Control & Monitor Interface and for the Host Request & Response protocols please refer to [3].

2.1.4 Address Select Inputs

The I^2C slave address of the coolteq.h™ Modulator can be selected from one of four pre-defined addresses, by the state of two external signals (3.3V CMOS). The actual addresses are programmable to accommodate customer requirements. For details please refer to [3].

2.1.5 nHostInt, Host Interrupt Output

The nHostInt output is a push-pull (3.3V CMOS) output line provides real-time notification of events, alarms and warnings as configured via the Control & Monitor Interface.

The following alarms/warnings can be monitored via nHostInt line:

- LVDS Clock Loss Alarm
- High Temperature Alarm/Warning
- Vsl and Vsh Low/High Alarm/Warning
- Va Low Warning
- Low Temperature Alarm/Warning
- System Alarm/Event

2.1.6 TDDPowerSave, TDD Mode Power Saving Signalling Input

This pin has been reserved to put the coolteq.h™ Modulator into TDD Power Save state for TDD mode uplink phase.

2.1.7 nResetIn, External Reset Input

nResetIn, the external reset input, pin has been reserved to reset the coolteq.h™ Modulator. nResetIn is a negative logic input to the to the coolteq.h™ Modulator. If an external reset control is not required for the coolteq.h™ Modulator, the nResetIn pin should be left unconnected.

2.1.8 nResetOut, Reset Indicator

The coolteq.h™ Modulator has supply voltage fault detection mechanism. When a supply voltage dropout is detected, the coolteq.h™ Modulator resets itself automatically. The nResetOut pin has been reserved to send a negative logic signal to indicate such reset occurred. The nResetOut pin becomes active when nResetIn pin is activated as well. If nResetOut pin is not utilised, it should be left unconnected

2.1.9 PA Drain Voltage Output

This output is intended to supply the drain of the RF amplifier device. For information on how to implement this connection please refer to [1].

2.2 Operation of coolteq.h™ Modulator

Figure 2 provides a conceptual model of the internal functionality of the coolteq.h™ Modulator. The input LVDS envelope signal is passed through a 2 X interpolation filter before being fed into a DAC. Although there are other contributing blocks, the frequency response of the coolteq.h™ Modulator is largely determined by this interpolation filter.

The output of the DAC is passed through a reconstruction filter creating the analogue reference signal for the output section of the Modulator; this output block can be conceptualised as a high power, high bandwidth and high efficiency operational amplifier.

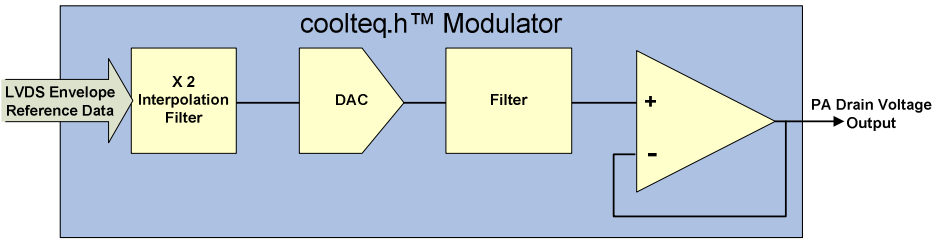

Figure 2. Model of coolteq.h™ Modulator Functionality

2.3 Safe Operating Area

The coolteq.h™ Modulator incorporates a protection mechanism called Safe Operating Area (SOA) that the coolteq.h™ Modulator shuts down when overload condition is detected. For information on how to identify an SOA event and how to restart the coolteq.h™ Modulator please refer to [3].

3 ET Amplifier System

3.1 Overview

Figure 3 shows the block diagram of a digital envelope tracking amplifier. When implementing an envelope tracking digital amplifier the following additional aspects have to be considered compared to conventional fixed drain systems:

- Envelope Reference Data has to be created for the coolteq.h™ Modulator (shaping) from the crest factor conditioned signal
- Control functionality for the coolteq.h™ Modulator has to be implemented (Control & Monitor Interface)
- A means of delay adjustment between the RF signal and the Envelope Reference Data has to be implemented

The following figure shows the major blocks of the envelope tracking digital amplifier.

Both the lower pre-distortion (DPD) signal path and the upper envelope reference signal path are fed from a common crest factor conditioned input signal.

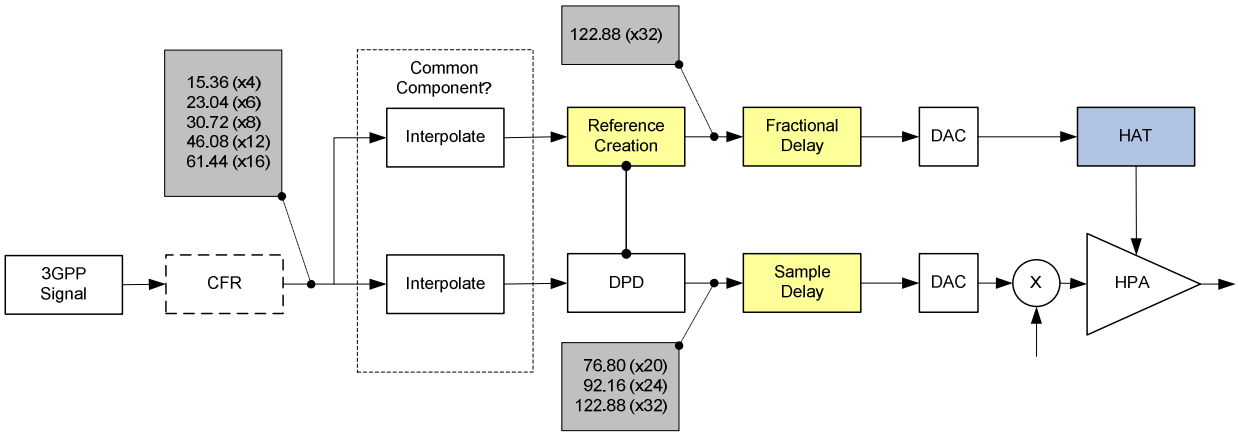

Figure 3. Block Diagram of Digital Envelope Tracking Amplifier

The coolteq.h™ Modulator is designed to accept a reference input of 122.88Msps which supports up to 50MHz of signal bandwidth. For 3GPP systems this signal input is typically generated from a composite multi-carrier signal of either 30.72Msps or 61.44Msps by a cascade of half band filters.

DPD solutions supporting 3 or more WCDMA carriers are typically found to operate with an input signal of 30.72, 46.08 or 61.44Msps and produce an output sample rate of 92.16 or 122.88 Msps. The 122.88Msps reference rate for the modulator may therefore be derived using a 4x, 8/3x, or 2x interpolation filter and, in the case of integer multiples, the interpolation filtering may be shared.

3.2 Envelope Reference Data Creation

Section 4.3 of the coolteq.h™ Modulator Design Guide [1] has introduced how the optimum Vdd – Pout points can be obtained for best efficiency based on measurements of the amplifier. A curve is fitted on these points to obtain the shaping function that provides a smooth transition between the minimum coolteq.h™ Modulator output voltage region at low RF power levels to the Active Drain Modulation region at higher power levels.

The steps to generate the Envelope Reference Data for the coolteq.h™ Modulator are shown in Figure 4 as an example for a coolteq.h™ Modulator with 10-28V output swing range.

1. Apply shaping function to the normalised baseband signal amplitude. This results in an analogue Envelope Reference with a range of 10V to 28V.
2. Digitize the analogue reference signal linearly, so that 10V corresponds to 0 and 28V to full scale (2^{14}-1) and output it to the coolteq.h™ Modulator on the LVDS Envelope Reference Data Interface.

The exact shaping function used has an influence on both distortion and efficiency. Figure 5 illustrates how a shaping function with a ‘sharper’ corner transition results in higher order distortions increasing the demand on the DPD block.

System level optimisation is required to find the shaping function that gives best trade-off between the efficiency and linearity requirements.

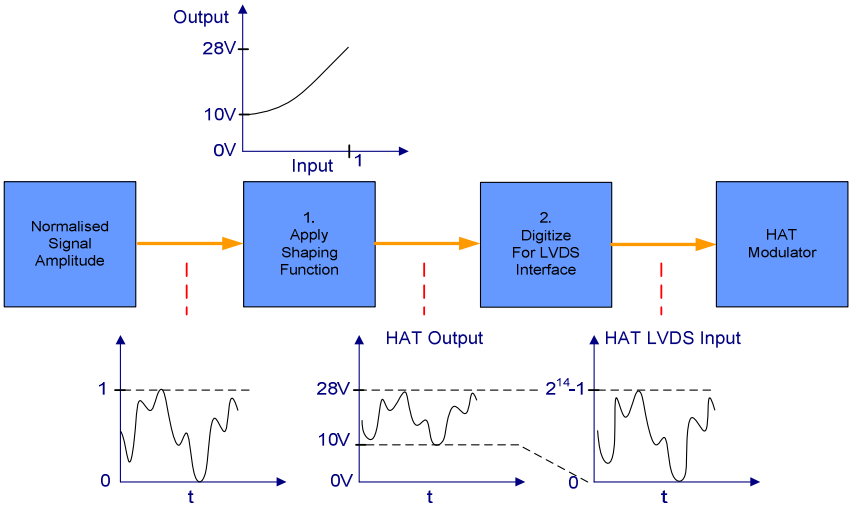

Figure 4. Steps of Envelope Reference Data Creation.

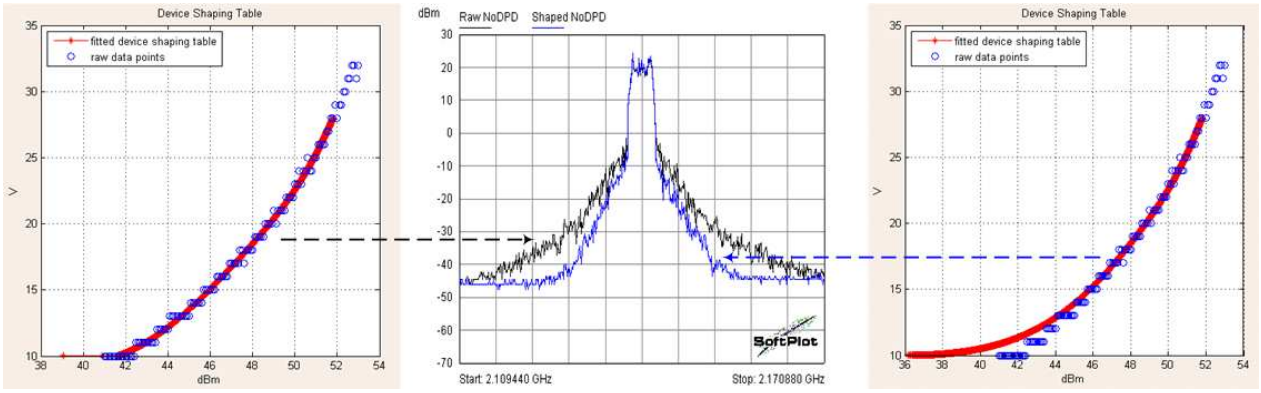

Figure 5. RF Spectrum versus Shaping Function

3.3 Timing Alignment

An important aspect of operating envelope tracking systems is providing accurate timing alignment of the drain supply waveform with the RF signal to be amplified. Misalignment of these waveforms will result in a strong 'memory effect' that may be difficult or impossible to linearise depending on the severity of the timing misalignment involved.

The accuracy with which timing alignment should be achieved is nominally a function of the bandwidth of the transmitted signal. For signals having bandwidths of 20MHz or greater, the ability to align to sub nanosecond resolutions is desirable.

To facilitate accurate timing alignment either the signal or drain reference path should include a fractional sample delay filter. To compensate the relative process delays of the individual signal processing paths and any associated analogue circuitry, an integer sample delay block may also be required in either the reference or DPD processing path. In **Figure 3** this delay is shown in the DPD path.

In a production system dynamic adjustment of the timing alignment is required to minimise distortion. This can be based upon analysis of the feedback signal used for DPD.

4 DPD Considerations for ET

With a conventional PA, both memory and memory-less nonlinearities are experienced as the PA moves into compression. Most of the memory effect occurs at the peaks of the waveform where the amplifier is most in compression. Envelope tracking modifies this behaviour as the amplifier will enter compression 6-8dB below the peak power point.

When implementing a DPD system using envelope tracking the following aspects have to be considered that are different from a DPD system used with fixed drain amplifiers:

- dAM/AM and dPM/AM characteristics of the PA can be very different from when operated in fixed drain configuration
- Depending on drain waveform, higher DPD bandwidth may be required due to the effect of drain voltage to phase modulation, particularly with LDMOS devices

4.1 dPM/AM Characteristics

The high phase modulation distortion component when using LDMOS devices is illustrated by **Figure 6**. It can be seen that although the initial distortion is quite high due to phase modulation, it can be easily linearised and even by the removal of the non memory distortion elements only, an ACP of -55dBc can be achieved.

4.2 dAM/AM Characteristics

The instantaneous gain of the envelope tracking power amplifier is determined by the Vdd selected at the current output power. As Vdd is changed corresponding to the output power the dAM/AM characteristics of an envelope tracking amplifier can be quite different compared to the typical compression like curve of a fixed drain amplifier. A GaN device for example may exhibit gain expansion with increasing output powers as the corresponding drain voltage is increased.

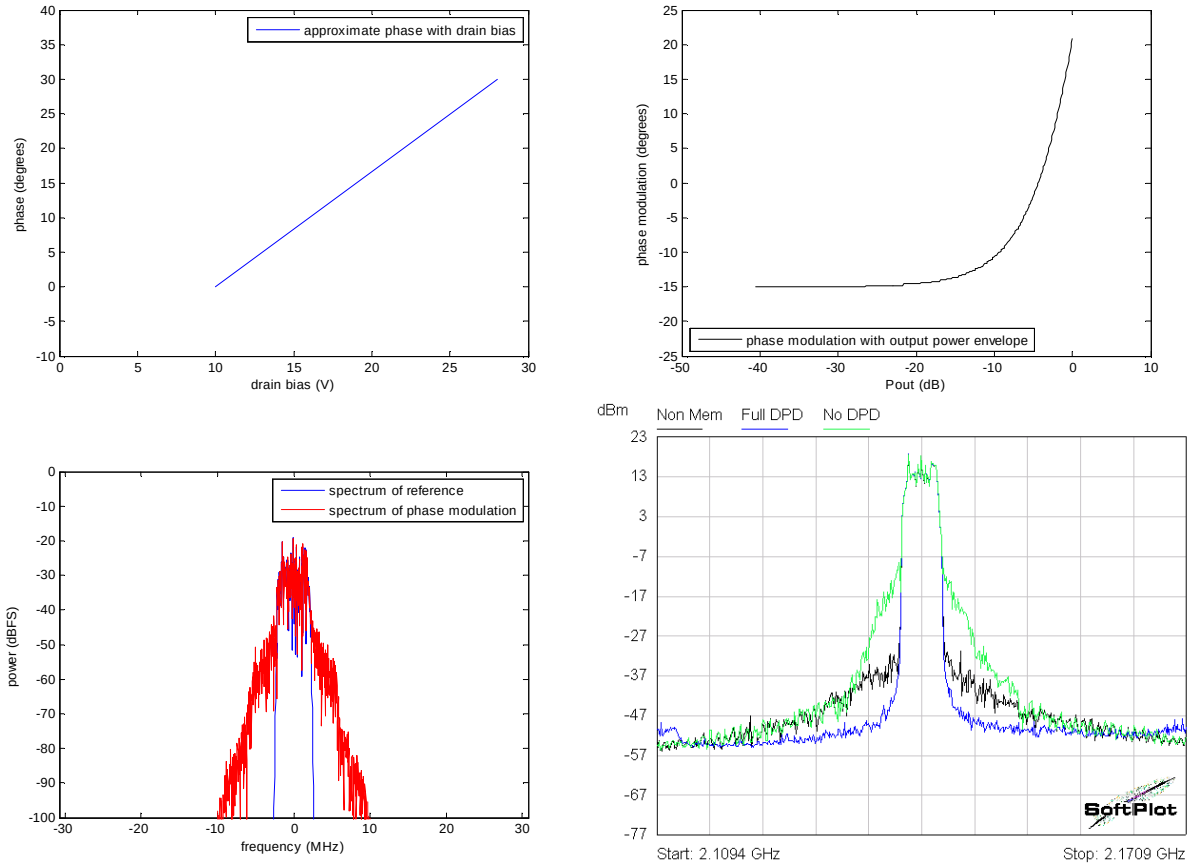

Figure 6. Simulated and Measured Distortion due to Phase Modulation of LDMOS device

5 TDD Mode Power Saving Utilisation

The coolteq.h™ Modulator supports TDD mode for WiMAX and WCDMA systems. The TDD Mode Power Saving operation is enabled and disabled using configuration requests via the coolteq.h™ Modulator Control and Monitoring interface. To activate the TDD mode of operation, please see details given in section 6.5 and refer to [3].

The coolteq.h™ Modulator provides two methods for a Baseband controller to utilise the TDD Mode Power Saving function.

1. LVDS Envelope Reference Data (in-band) signalling through the coolteq.h™ Modulator Envelope, Control & Monitor connector.
2. Dedicated TDD Mode Power Saving signalling pin (TDDPowerSave) on the coolteq.h™ Modulator Envelope, Control & Monitor connector.

5.1 coolteq.h™ Modulator Power Saving Settling Time

The coolteq.h™ Modulator has ~65µs Power Saving Settling Time to switch PA drain output from normal modulation level to 0V Power Saving level. During PA Drain Voltage Modulation, the coolteq.h™ Modulator PA Drain Output voltage level does not go down below Vmin level. During Power Saving state, the coolteq.h™ Modulator PA Drain Output voltage level drops to 0V. The coolteq.h™ Modulator Power Saving Settling Time is depicted in **Figure 7**.

5.2 coolteq.h™ Modulator Recovery Time from Power Saving

The coolteq.h™ Modulator has ~65µs Recovery time to switch from Power Saving state to normal PA Drain Voltage Modulation level. Therefore, the Host should deactivate TDD Mode Power Saving function at least 65µs prior to the RF Transmit. The coolteq.h™ Modulator Power Saving Recovery Time is depicted in **Figure 7**.

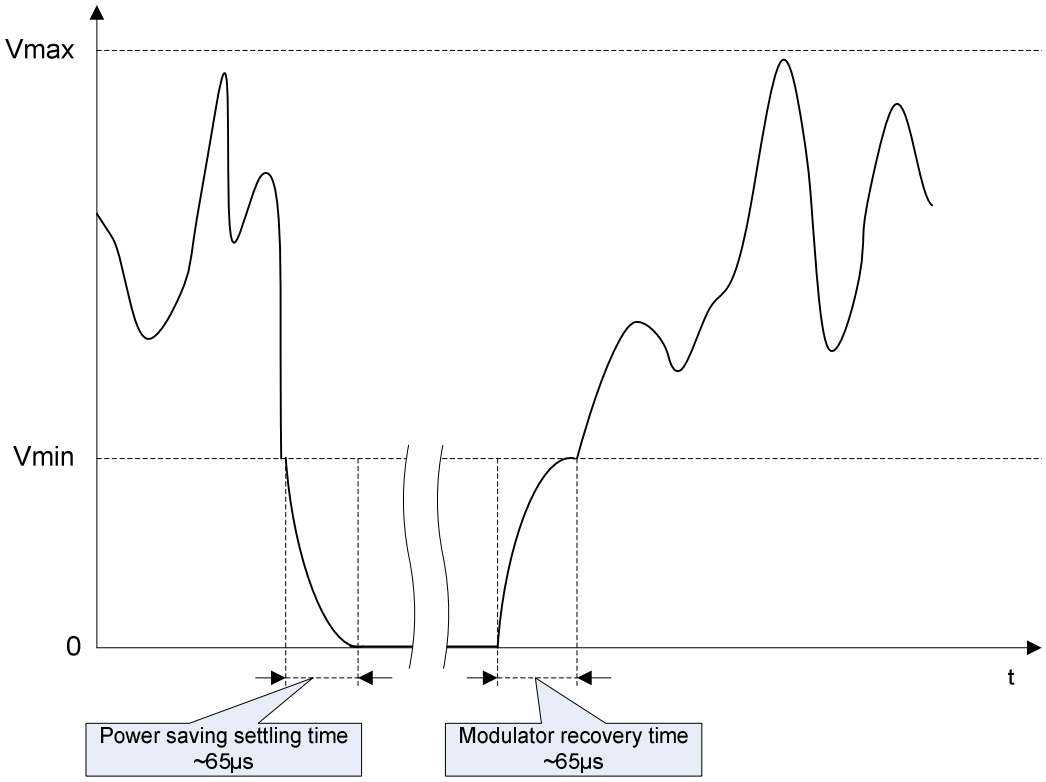

Figure 7. The coolteq.h™ Modulator PA Drain Output During Power Saving

5.3 TDD Mode Power Saving with LVDS Envelope Reference Data Signalling

When TDD Mode Power Saving function enabled for LVDS Envelope Reference Data (in-band) signalling, 50(fifty) consecutive reading of LVDS Envelope Reference Data with value equal to or less than 3 will put the coolteq.h™ Modulator into TDD Power Saving state. The coolteq.h™ Modulator stays in TDD Power Saving state as long as LVDS Envelope Reference Data values less than or equal to 3. Any 5 (five) consecutive LVDS Envelope Reference Data with value greater than 3 will make coolteq.h™ Modulator switch to normal PA Drain voltage Modulation. LVDS Envelope Reference Data with embedded Power Saving code is depicted in **Figure 8**.

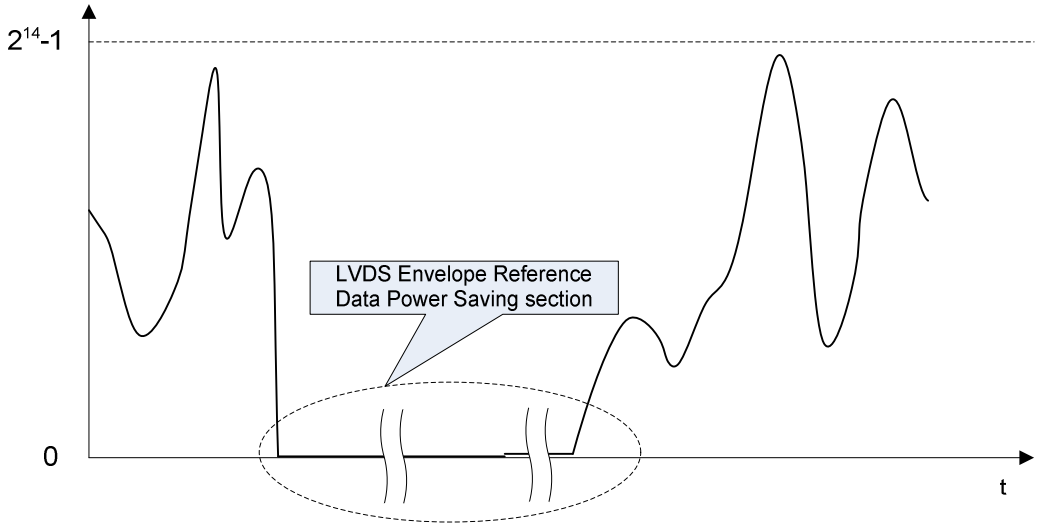

Figure 8. Power Saving on LVDS Envelope

To keep the coolteq.h™ Modulator in TDD Power Saving state, the Host should continue to send LVDS Envelope Reference Data value ≤3.

The coolteq.h™ Modulator has ~65µs settling time to switch from Power Saving state to normal PA Drain Voltage Modulation. Therefore, the Host should apply LVDS Envelope Reference Data value >3 to switch the coolteq.h™ Modulator into normal operation at least 65µs prior to actual LVDS envelope. A detailed depiction of LVDS Envelope Reference Data for Power Saving operation is given in **Figure 9**.

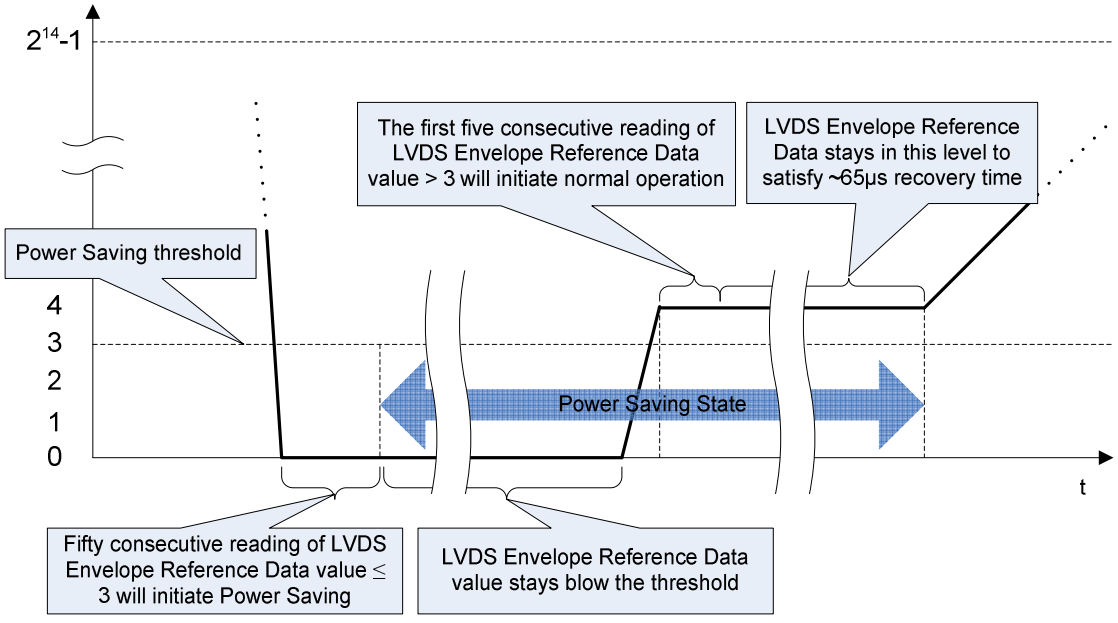

Figure 9. Detailed view of LVDS Envelope Reference Data for Power Saving

5.4 TDD Mode Power Saving with TDD Mode Power Saving (TDDPowerSave) Pin Signalling

The HAT™ Modulator's TDD Mode Power Saving signalling pin (TDDPowerSave) is a positive logic input to put the HAT™ Modulator into TDD Power Saving state. When TDD Mode Power Saving function enabled for TDD Mode Power Saving signalling pin (TDDPowerSave), the HAT™ Modulator immediately goes into TDD Power Saving state. The coolteq.h™ Modulator stays in TDD Power Saving state as long as TDDPowerSave pin is active.

The Power Saving Settling and Recovery from Power Saving duration should be taken into consideration when TDDPowerSave pin is signalled. LVDS Envelope Reference Data value should be kept its minimum level (0) through out the TDD Power Saving state. Detailed depiction of PA Drain Voltage Output, LVDS Reference Envelope Data and TDDPowerSave pin level are given in **Figure 10**.

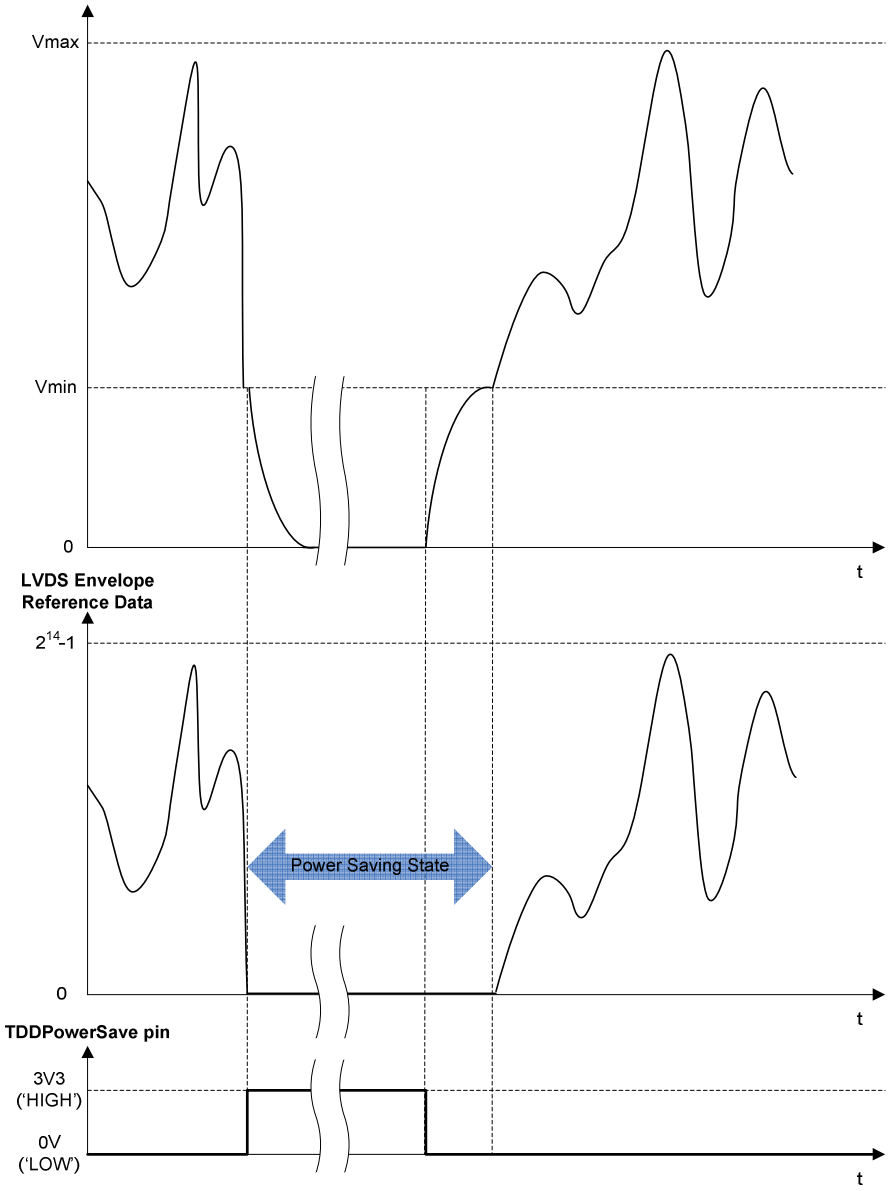

Figure 10. TDD Power Save Pin Signalling

6 coolteq.h™ Modulator Control and Monitoring

A typical coolteq.h™ Modulator Control & Monitor Interface connection diagram is given in the **Figure 11**. In the figure, the Host monitors the coolteq.h™ Modulator via nHostInt interrupt line, and interacts with the coolteq.h™ Modulator using the coolteq.h™ Modulator Control & Monitor Interface Protocol through I^2C connection. Utilisation of the nHostInt line is dependent upon the system design. The Host might use a polling based control scheme in which nHostInt line might be polled.

The nResetIn line is utilised to reset the coolteq.h™ Modulator by the Host. Utilisation of the nResetOut line is dependent upon the system design. The Host might poll the nResetOut line to detect if the coolteq.h™ Modulator is reset due to a fault detection.

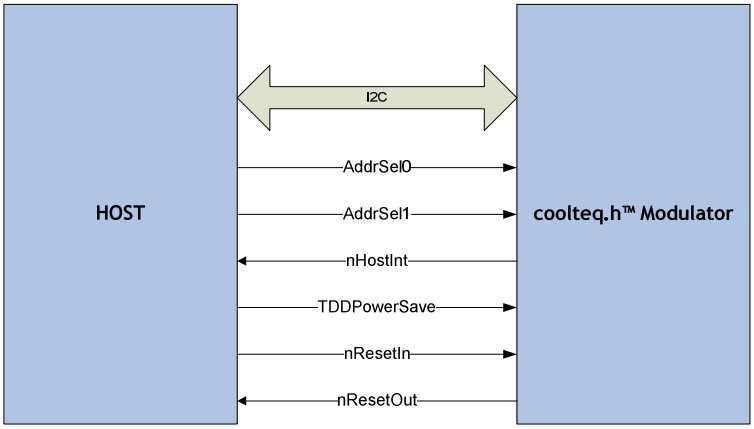

Figure 11. coolteq.h™ Modulator Control & Monitor Interface

6.1 coolteq.h™ Modulator Operating Modes

The HAT™ Modulator runs in one of the two operating modes; Modulation Mode and Maintenance Mode. The native operating mode of the HAT™ Modulator is Modulation Mode. Therefore, the HAT™ Modulator starts working in Modulation Mode after a reset or a power-on.
The HAT Modulator can only switch to Maintenance Mode if the Host send an EnterMaintenanceMode command. The HAT™ Modulator switches back to Modulation Mode if the Host sends an ExitMaintenanceMode command.

1. **Modulation Mode**: HAT™ Modulator's normal operational mode.
   The HAT™ Modulator can communicate to the Host.
   The HAT™ Modulator always returns to Modulation Mode automatically after a reset.
   Configuration parameters cannot be changed in Modulation Mode.
   SW/FW cannot be downloaded into the HAT™ Modulator in Modulation Mode.
   The HAT™ Modulator can switch from one configuration set to another as a result of a Host request.
   Depending on the configuration, PA Drain Voltage Modulation is started automatically if there is no alarm (fault) condition.
2. **Maintenance Mode**:
   The HAT™ Modulator can communicate to the Host.
   Configuration parameters and configuration sets are manipulated in Maintenance Mode.
   The HAT™ Modulator cannot provide PA Drain Voltage Modulation in Maintenance Mode.
   SW/FW can be downloaded into the HAT™ Modulator in Maintenance Mode.

6.2 Automatic PA Drain Voltage Modulation

After a reset or a power on, the HAT™ Modulator directly goes into the Modulation Mode. Depending on the configuration set, the PA Drain Voltage Modulation can start automatically if the operation conditions are met i.e. there are not any alarm conditions.

It is possible to disable the Automatic PA Drain Voltage Modulation feature in the configuration sets.

The Host (Baseband Controller) can stop PA Drain Voltage Modulation as well as disable Automatic PA Drain Voltage Modulation feature using appropriate commands if required. However, after a reset or a power cycle, the current configuration set can enable Automatic PA Drain Voltage Modulation feature.

If Automatic PA Drain Voltage Modulation is enabled, the HAT™ Modulator continuously monitors operation conditions, raise or remove alarms/warnings and clears internal status bits automatically.

6.3 coolteq.h™ Modulator's Behavioural Finite State Machine

coolteq.h™ Modulator's application level actions are depicted in the Finite State Machine diagram given in **Figure 12**. The coolteq.h™ Modulator is an event driven system. Events are generated by internal processes, HW blocks as well as by the Host with Host Requests through Control & Monitor Interface via I^2C connection.

After a power up the coolteq.h™ Modulator FW initialises the modulator HW and starts house keeping, status monitoring (for alarms and warnings) and host communication (through I2C interface) activities. Warnings are monitored concurrently. Warnings do not interfere with PA Drain Voltage Modulation operation. Alarms, on the other hand, stop ongoing PA Drain Voltage Modulation or prevent the coolteq.h™ Modulator starting PA Drain voltage Modulation until the alarm conditions are removed and alarm status bits are cleared. coolteq.h™ Modulator's Watch Dog Timer or Power Supply Fault Detection HW blocks can reset the coolteq.h™ Modulator if a power supply drop out or a FW lock up are detected.

The coolteq.h™ Modulator can start PA Drain voltage Modulation automatically after power-up or reset events if Automatic PA Drain Voltage Modulation option is enabled.

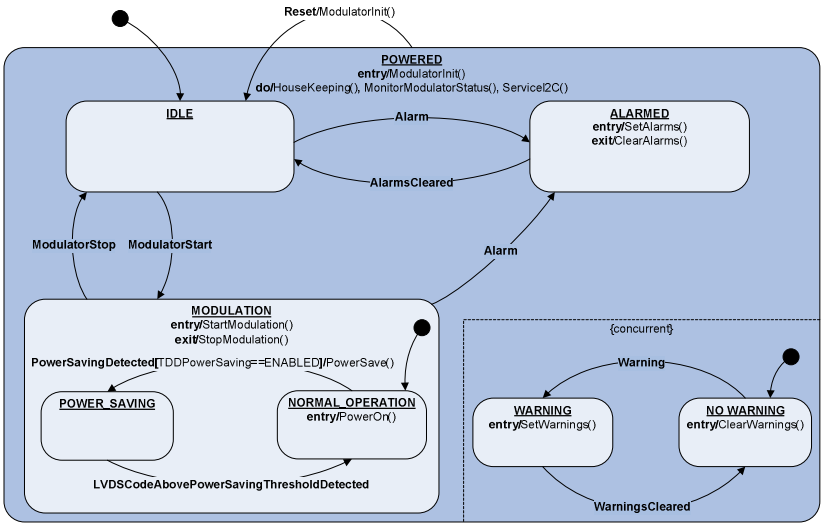

Figure 12. coolteq.h™ Modulator Finite State Machine

6.4 coolteq.h™ Modulator Start-up

Prior to starting the coolteq.h™ Modulator's standard operation, certain initial and operating conditions need to be satisfied. These conditions generally controlled and maintained by the Host. A typical coolteq.h™ Modulator start-up sequence is given in **Figure 13**. During the start-up sequence, the Host turns on the main and auxiliary supplies and establishes the I^2C link to the coolteq.h™ Modulator. If the coolteq.h™ Modulator has a connection or an internal fault, the situation can be detected as an I^2C transaction error or by checking the Fatal Error bit in the MAIN_STATUS register. In both cases, the Host might use a power cycle sequence or applying reset signal to the nResetIn line for a recovery. Otherwise, the Host might start initialisation of the coolteq.h™ Modulator.

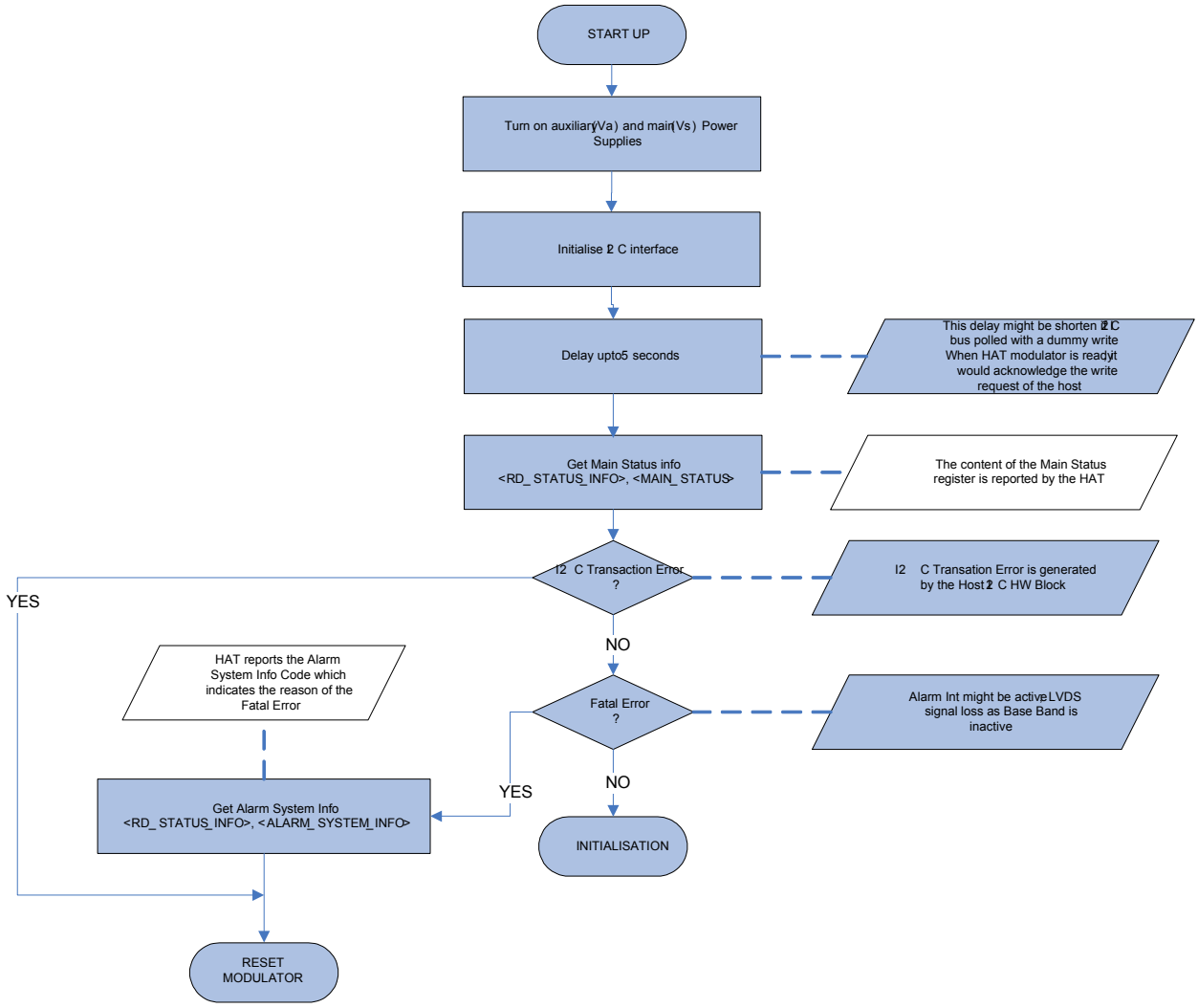

Figure 13. coolteq.h™ Modulator start-up

6.5 coolteq.h™ Modulator Initialisation

The coolteq.h™ Modulator needs to be initialised based on system requirements prior to modulation start. The Host might also need to get some attributes of the coolteq.h™ Modulator to use in the system level. A typical coolteq.h™ Modulator initialisation flow executed by the Host is given in the **Figure 14**.

Please note that initially a constant LVDS = 0 code should be applied to the modulator envelope input. Modulated LVDS signal should only be applied after the modulator has been started up successfully (see next section).

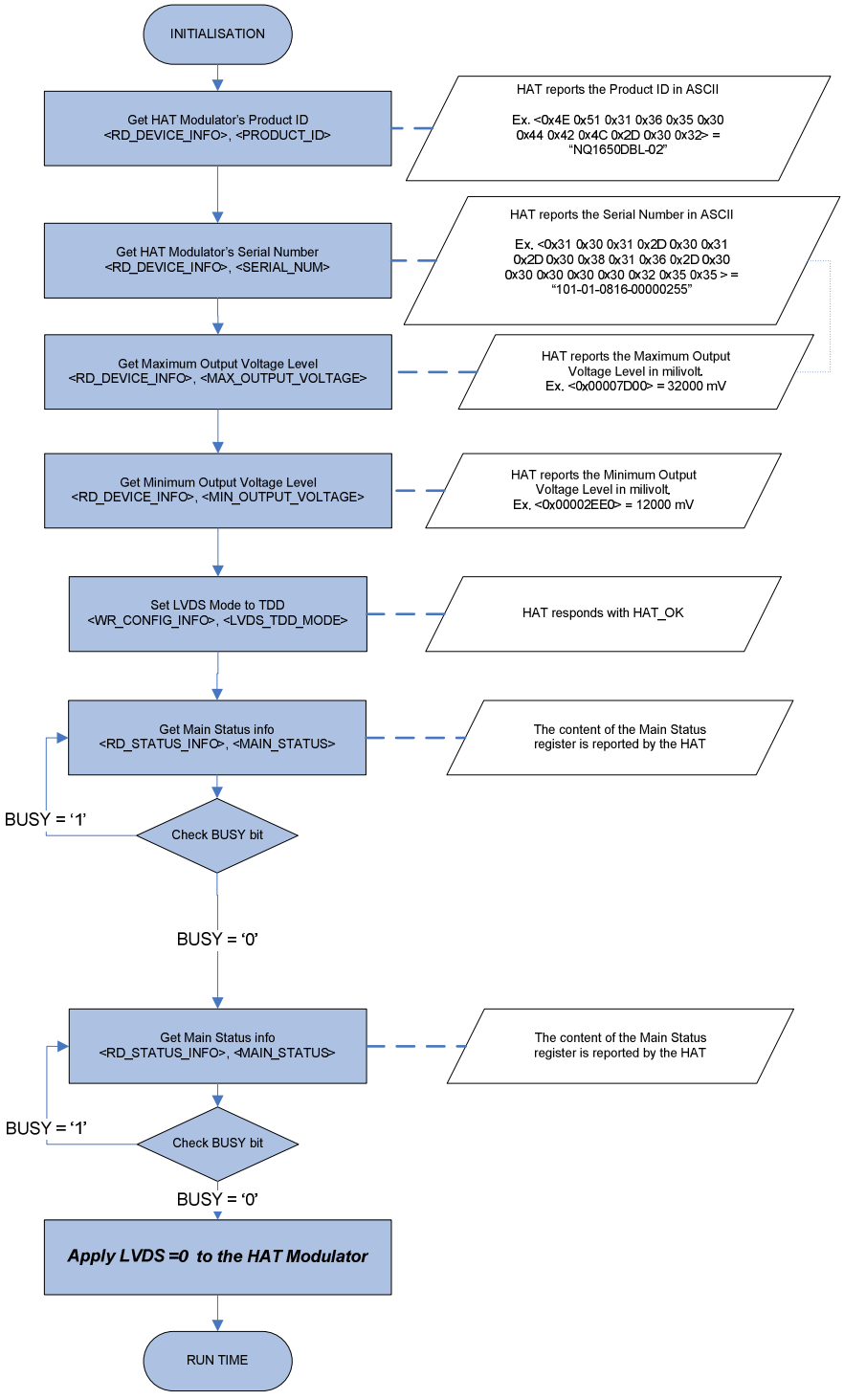

Figure 14. coolteq.h™ Modulator initialisation flow

6.6 coolteq.h™ Modulator at run-time

Standard mode of operation of coolteq.h™ Modulator can be observed during run-time. During run-time, the Host needs to monitor Warnings and Alarms following either event-driven or polling schemes, through HOST_INT interrupt line or using I^2C Interface Request & Response respectively. A polling based control flow is depicted in the **Figure 15**. Alarm and warning registers are cleared prior to entering the polling loop.

As, alarms and warnings might be fired up in start-up stage due to transient power supply or temperature levels, alarms and warning need to be cleared up by the Host.

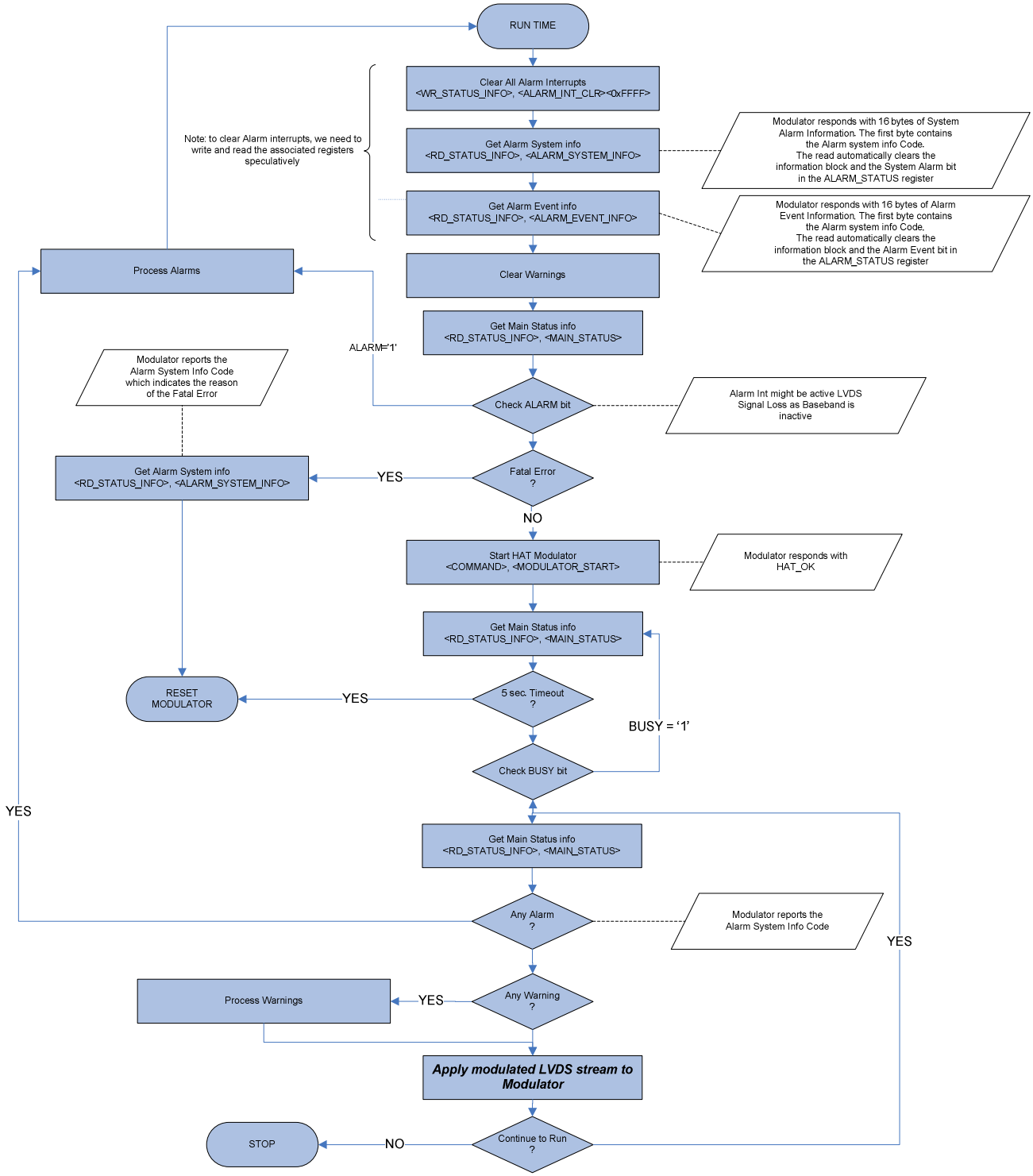

Figure 15. **coolteq.h™ Modulator control flow during run-time**

6.7 Stopping coolteq.h™ Modulator

The Host might require stopping the coolteq.h™ Modulator to change operation parameters or just to stop transmission. The **Figure 16** depicts required action taken by the Host to stop the coolteq.h™ Modulator. The Host checks the BUSY bit of MAIN_STATUS register and ensures that coolteq.h™ Modulator has completed the MODULATOR_STOP command.

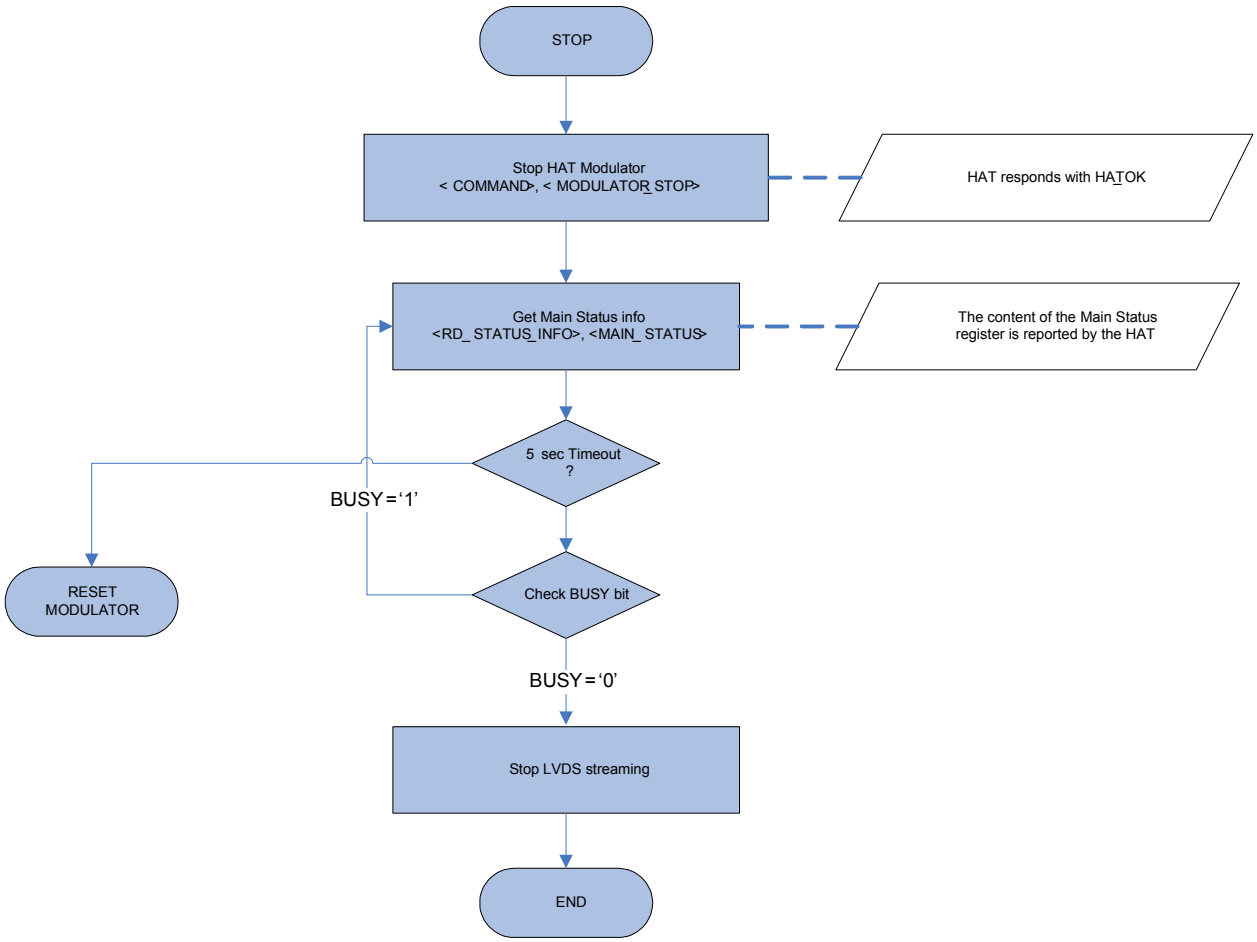

Figure 16. Process flow for the coolteq.h™ Modulator stop

6.8 Alarm Processing

When an Alarm condition occurs such as high temperature, extreme voltage levels in main and/or auxiliary supplies, LVDS clock loss, the coolteq.h™ Modulator stops automatically as alarms are considered as faults which prevent the coolteq.h™ Modulator operates in Safe Operating Area (SOA).

The coolteq.h™ Modulator provides detailed information for the alarms. This information might be acquired and processed by the Host. If the Host resolves the fault(s) caused the alarm(s), the coolteq.h™ Modulator might be re-started.

A typical alarm processing control flow is given in the **Figure 17**.

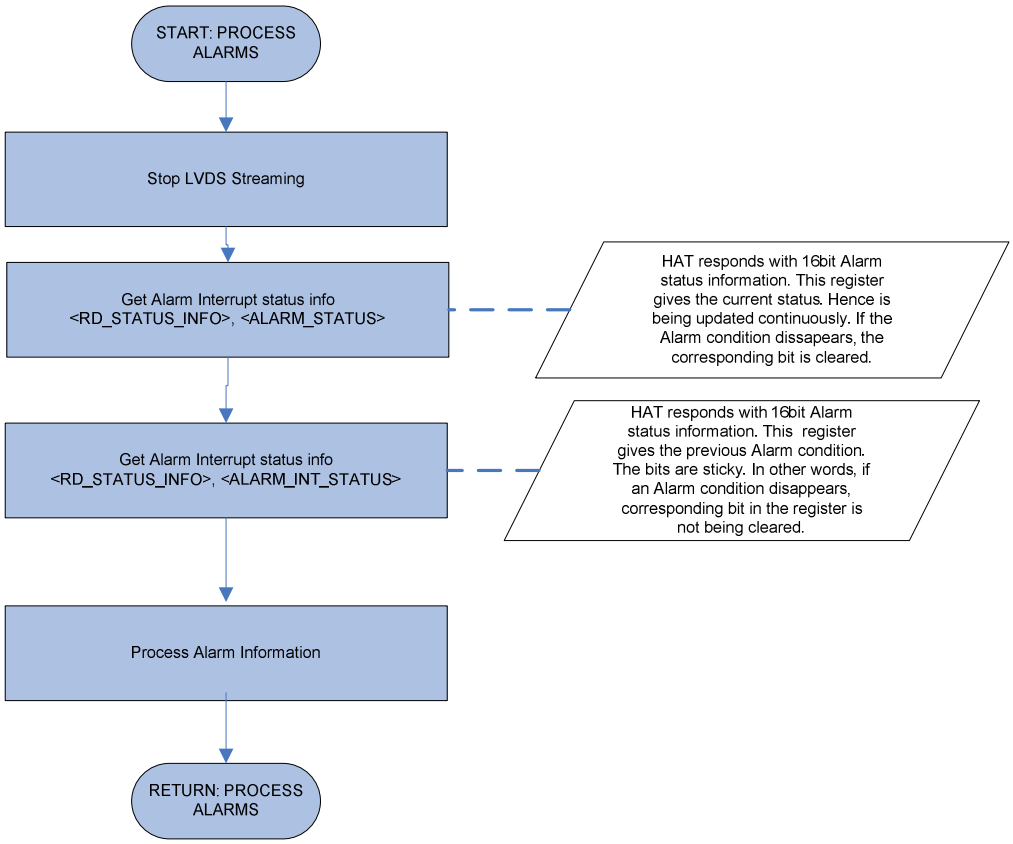

Figure 17. Alarm processing flow

6.9 Warning Processing

Warnings are utilised to indicate changing operating conditions and potential alarm conditions which might arise. Warnings do not prevent the coolteq.h™ Modulator's normal operations. However, they need to be processed by the Host carefully as they might lead to an alarm condition at which the coolteq.h™ Modulator stops.

A typical warning processing control flow is given in the **Figure 18**.

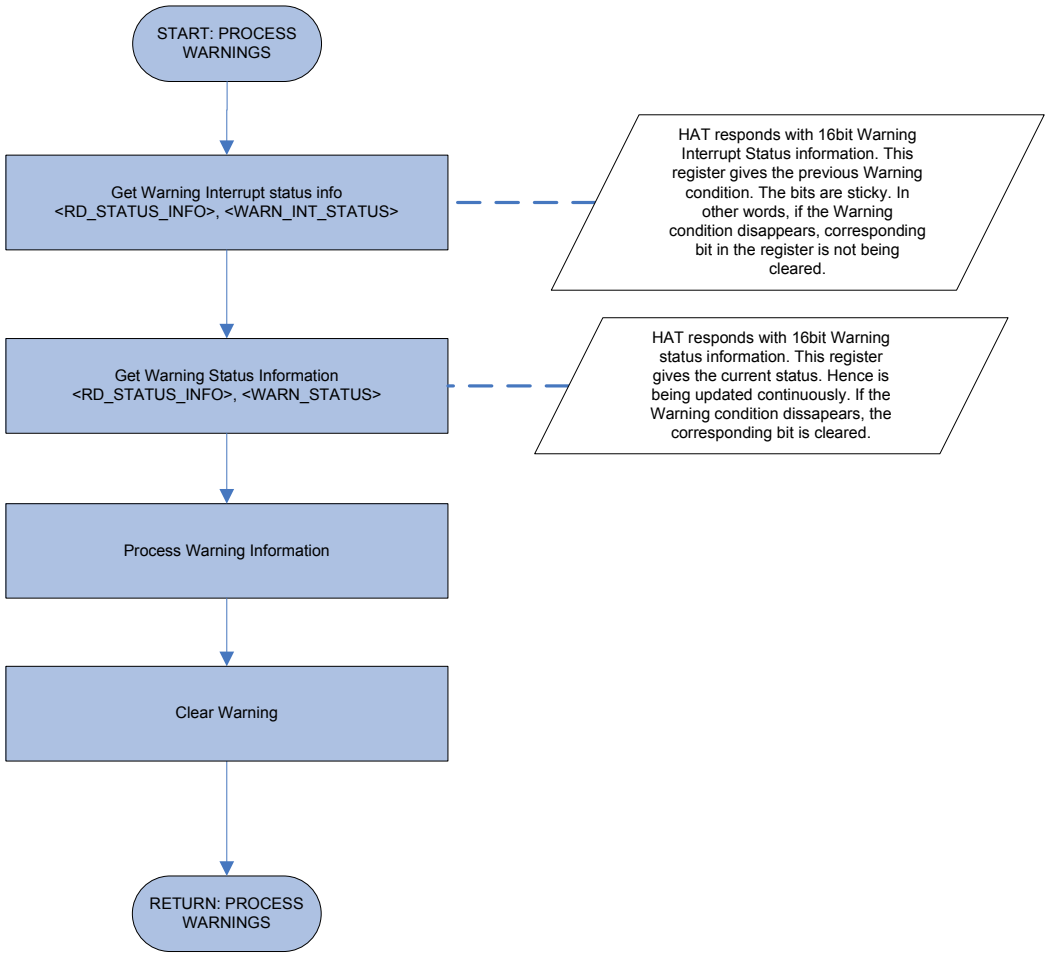

Figure 18. Warning processing flow

6.10 Clearing Warnings

Detailed information (System Info Code) about warnings might be gathered from WARN_SYSTEM_INFO and WARN_EVENT_INFO registers. Reading these registers can automatically clear these registers. The Host needs to clear up Warnings even though it doesn't require the contents.

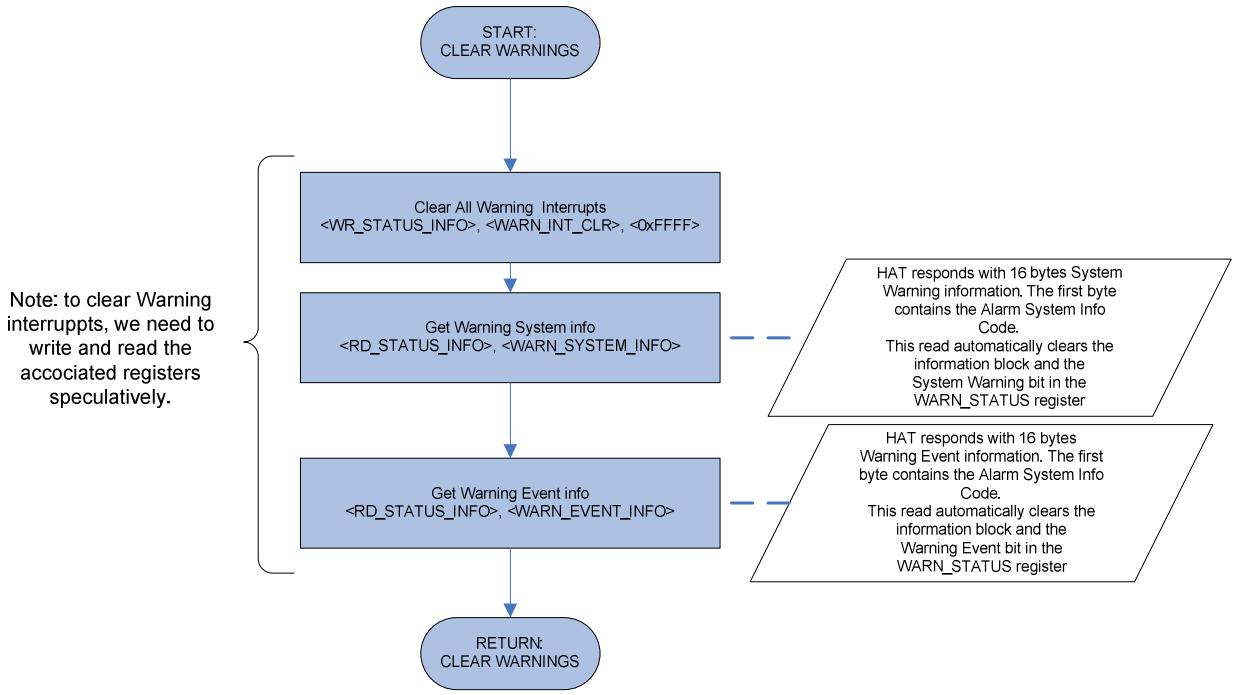

Figure 19. Clearing Warnings

7 References

[1] coolteq.h™ Modulator Design Guide, AN002077, Nujira Ltd.

[2] NCT-H4010 / N3009 coolteq.h™ Modulator Datasheets, PD002236 / PD002443 Nujira Ltd.

[3] Version 3 Control and Monitoring Interface, PD002239, Nujira Ltd.

[4] The I^2C Specification, version 2.1, January 2001, Philips Doc No 9398 393 40011.

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