1 Applications

High efficiency Envelope Tracking (ET) Power Amplifiers

- Wireless infrastructure: LTE, WCDMA, MC-GSM, CDMA, GSM (Multi-band, Multi-mode)
- Terrestrial television: DVB-T, ATSC, DTMB, ISDB
- Communication: LMDS/MMDS, point-to-point
- Pulsed radar
- Typically 20 W to 60 W average output power PAs

2 Features

- RF frequency agnostic
- Up to 20 MHz RF bandwidth for 20 MHz LTE or 4-channel WCDMA
- 6 to 12 dB PAPR supported
- LVDS envelope input
- I^2C control and configuration interface
- Built-in overload protection
- Temperature range from -25°C to +80°C
- Direct applications support for telecoms grade power input
- Open collector status indication
- 5 V-tolerant reset input
- Open collector reset output

3 General Description

The NCT-H4010 is a High Accuracy Tracking (HAT®) envelope tracking power modulator which provides the power supply to the output transistor in high efficiency ET RF power amplifiers.

The desired modulation waveform is fed to the modulator through a digital LVDS interface and is accurately replicated on the drain/collector of the PA transistor, thereby minimising supply-related memory effects.

The NCT-H4010 is typically used with 20 W to 60 W average Pout single-ended PAs, providing excellent results when operated in conjunction with Crest Factor Reduction (CFR) and Digital Pre-Distortion (DPD) baseband linearisation.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

4 Functional Block Diagram

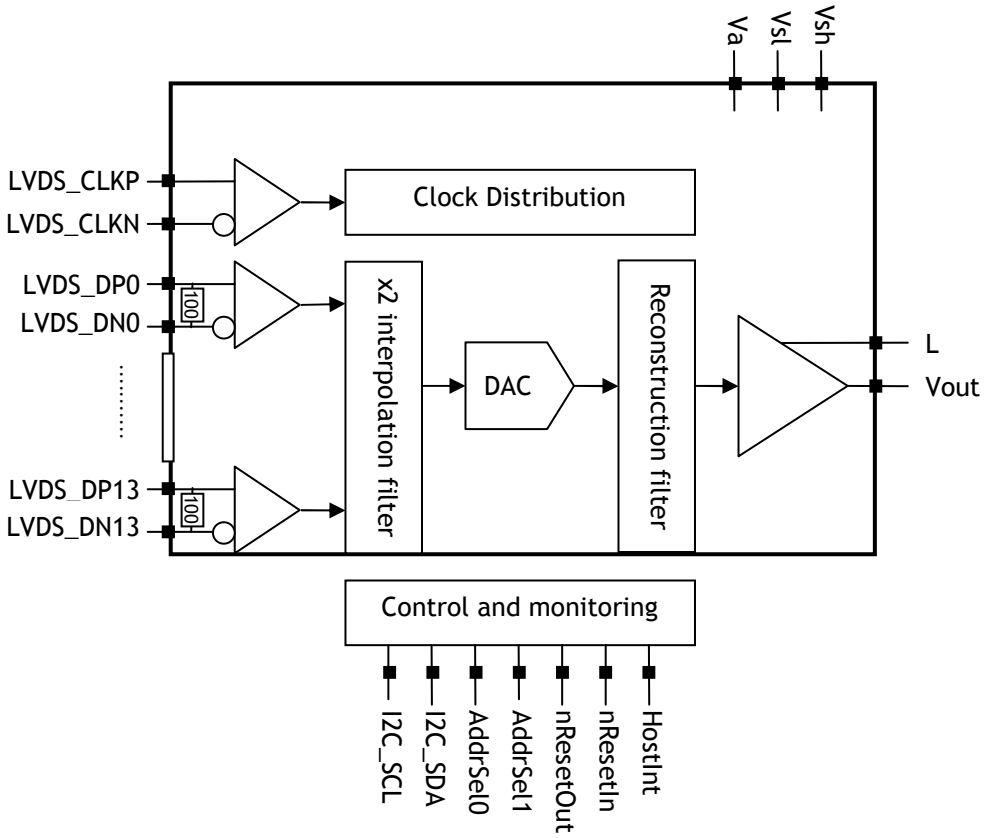


Figure 1: NCT-H4010 Functional Block Diagram

5 Terminal Descriptions

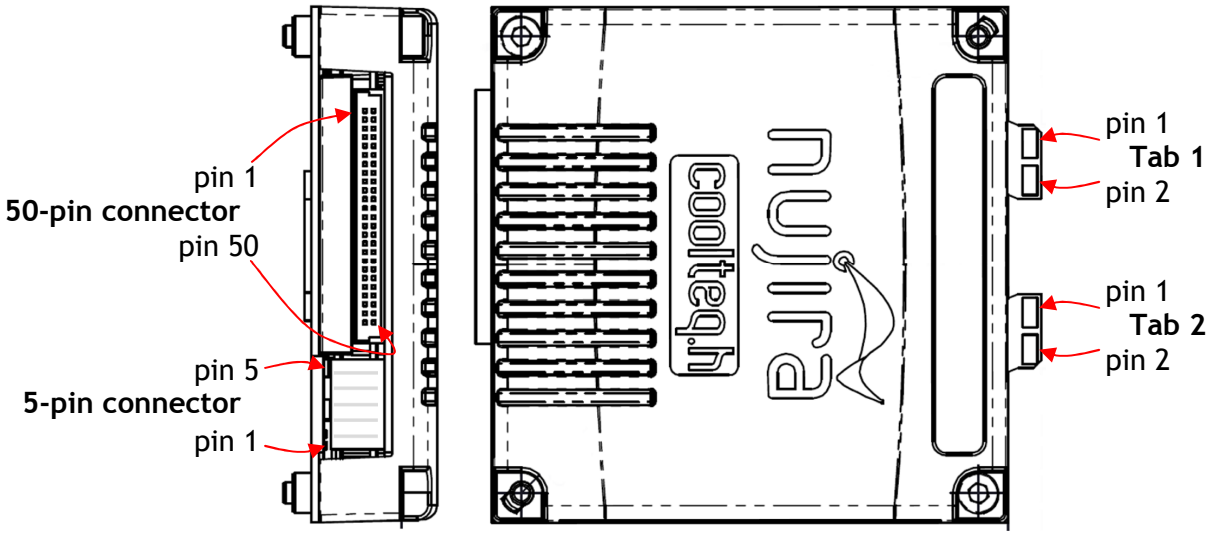


Figure 2: Terminal Description

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

5.1 LVDS Interface

SYMBOL	I/O	LOCATION	PIN	TYPE	DESCRIPTION
AddrSel0	I	50 pin connector	1	LVCMOS	I^2C address configuration
GND	-	50 pin connector	2	-	Ground
AddrSel1	I	50 pin connector	3	LVCMOS	I^2C address configuration
I2C_SCL	I+O	50 pin connector	4	I^2C	I^2C serial clock
GND	-	50 pin connector	5	-	Ground
I2C_SDA	I+O	50 pin connector	6	I^2C	I^2C serial data
nHostInt	0	50 pin connector	7	OD	Alarm and Warning status signal
GND	-	50 pin connector	8	-	Ground
GND	-	50 pin connector	9	-	Ground
GND	-	50 pin connector	10	-	Ground
LVDS_CLKP	I	50 pin connector	11	LVDS	LVDS data clock positive
LVDS_CLKN	I	50 pin connector	12	LVDS	LVDS data clock negative
GND	-	50 pin connector	13	-	Ground
GND	-	50 pin connector	14	-	Ground
LVDS_DP0	I	50 pin connector	15	LVDS	Data bit 0 negative
LVDS_DN0	I	50 pin connector	16	LVDS	Data bit 0 positive
LVDS_DP1	I	50 pin connector	17	LVDS	Data bit 1 negative
LVDS_DN1	I	50 pin connector	18	LVDS	Data bit 1 positive
LVDS_DP2	I	50 pin connector	19	LVDS	Data bit 2 negative
LVDS_DN2	I	50 pin connector	20	LVDS	Data bit 2 positive
LVDS_DP3	I	50 pin connector	21	LVDS	Data bit 3 negative
LVDS_DN3	I	50 pin connector	22	LVDS	Data bit 3 positive
LVDS_DP4	I	50 pin connector	23	LVDS	Data bit 4 negative
LVDS_DN4	I	50 pin connector	24	LVDS	Data bit 4 positive
GND	-	50 pin connector	25	-	Ground
GND	-	50 pin connector	26	-	Ground
LVDS_DP5	I	50 pin connector	27	LVDS	Data bit 5 negative
LVDS_DN5	I	50 pin connector	28	LVDS	Data bit 5 positive
LVDS_DP6	I	50 pin connector	29	LVDS	Data bit 6 negative
LVDS_DN6	I	50 pin connector	30	LVDS	Data bit 6 positive
GND	-	50 pin connector	31	-	Ground
GND	-	50 pin connector	32	-	Ground
LVDS_DP7	I	50 pin connector	33	LVDS	Data bit 7 negative
LVDS_DN7	I	50 pin connector	34	LVDS	Data bit 7 positive
LVDS_DP8	I	50 pin connector	35	LVDS	Data bit 8 negative
LVDS_DN8	I	50 pin connector	36	LVDS	Data bit 8 positive
GND	-	50 pin connector	37	-	Ground
GND	-	50 pin connector	38	-	Ground
LVDS_DP9	I	50 pin connector	39	LVDS	Data bit 9 negative
LVDS_DN9	I	50 pin connector	40	LVDS	Data bit 9 positive
LVDS_DP10	I	50 pin connector	41	LVDS	Data bit 10 negative
LVDS_DN10	I	50 pin connector	42	LVDS	Data bit 10 positive
LVDS_DP11	I	50 pin connector	43	LVDS	Data bit 11 negative
LVDS_DN11	I	50 pin connector	44	LVDS	Data bit 11 positive
LVDS_DP12	I	50 pin connector	45	LVDS	Data bit 12 negative
LVDS_DN12	I	50 pin connector	46	LVDS	Data bit 12 positive
LVDS_DP13	I	50 pin connector	47	LVDS	Data bit 13 negative
LVDS_DN13	I	50 pin connector	48	LVDS	Data bit 13 positive
nResetOut	O	50 pin connector	49	OD	Reset indicator output, active LOW
nResetIn	I	50 pin connector	50	LVCMOS	Reset input, active LOW

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

5.2 5-Pin Connector

SYMBOL	I/O	LOCATION	PIN	TYPE	DESCRIPTION
Va	I	5 pin connector	1	Power	3.3 V auxiliary power supply
Vsl	I	5 pin connector	2	Power	24 V main supply 1
Vsh	I	5 pin connector	3	Power	48 V main supply 2
GND	-	5 pin connector	4	-	Power supply ground
GND	-	5 pin connector	5	-	Power supply ground

5.3 Tabs

SYMBOL	I/O	LOCATION	PIN	TYPE	DESCRIPTION
Vout	O	Tab 1	1		Modulated drain power feed
GND	-	Tab 1	2	-	-
L	O	Tab 2	1		Bypass inductor power feed
GND	-	Tab 2	2	-	-

6 Limiting Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{sh}	Main supply 2	-0.5	70	V
V_{sl}	Main supply 1	-0.5	35	
V_a	Auxiliary power supply	-0.5	3.6	
LVDS_CLKP/N, LVDS_DP/Nxx	LVDS Interface	-0.5	3.0	V
I2C_SCL, I2C_SDA	I^2C Interface	-0.5	3.6	V
nHostInt	Alarm / Warning Status Signal (Host Interrupt) Interface voltage	-0.5	5.5	V
	Alarm / Warning Status Signal (Host Interrupt) Interface max current	-	20	mA
nResetOut	Hardware reset input voltage range	-0.5	5.5	V
V_{out}	Vout (PA drain voltage output) short circuit duration	0	Indefinite	s
T_{amb}	Operating temperature range (modulator baseplate)	-25	+80	°C
T_{stg}	Storage temperature range	-40	+100	°C

Stress in excess of Limiting Ratings may cause permanent damage. Limiting ratings are normally tested with one parameter at a time exceeding the limits of Electrical Characteristics. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

7 Electrical Characteristics

(Standalone modulator $T_{baseplate}$ = 25°C, R_L = 6.5Ω, Vout = 25-65V, Shaping = Wilson on given Test Circuit unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS	TEST	MIN	TYP	MAX	UNIT
DC Power Supply Input Requirements[1]							
V_{sh}	Main supply 2 voltage range		I	44	48	60	V
	Supply capacity requirement	for full power	-	180	-	-	W
	Peak transient current	10µs at 48V	I	7.5	-	-	A
V_{sl}	Main supply 1 voltage range		I	23	24	35	V
	Supply capacity requirement	for full power	-	50	-	-	W
	Peak transient current	10 µs at 24 V	I	7.5	-	-	A
V_a	Auxiliary supply voltage		I	3.135	3.3	3.465	V
	Supply capacity requirement		-	-	1	-	W
	Peak transient current	10 µs at 3.3 V	I	300	-	-	mA
LVDS Envelope Reference Data Interface Bus Characteristics[2]							
	Data and clock speed[3]			105	122.8	125	MHz
LVDS_CLKP/NLVDS_DP/Nxx	Common Mode Voltage (V_{CM})	compliant with ANSI/TIA/EIA-644		$\|V_{ID}\|/2$	-	2.4-$\|V_{ID}\|/2$	V
	Input Differential Voltage (V_{ID})			0.1	-	0.6	V
	LVDS_DP/N[0-13] Stable to LVDS_CLKP/N Low (Setup) (Tsu)			3			ns
	LVDS_CLKp/n Low to LVDS_Dp/n[0-13] Change (Hold) (Thd)			2			ns
LVDS_CLKP/N	Clock Period (Tpd)			8	8.138	9.524	ns
	Tolerance to clock jitter			-	-	120	ps
Control and monitoring interface characteristics							
AddrSel0/1, nResetIn	V_{IL}, Input Low Voltage			0	-	0.8	V
	V_{IH}, Input High Voltage			2.0	-	3.3	V
nHostInt	V_{OCOL}, OC Output Low Voltage			-	-	0.4	V
	$I_{O,}$ Output current				4		mA
	short-circuit current					45	mA
nResetOut	V_{OCOL}, OC Output Low Voltage			-	-	0.3	V
	$I_{O,}$ Output current				20		mA
	short-circuit current					200	mA

[1] Design verification tests have been carried out with Vsl and Vsh pairings of 23/44V, 28/48V and 35/60V, supply rails should be constrained to similar pairings, for example, depending on waveform characteristics, it may not be acceptable to have Vsl = 35V and Vsh=44V. Refer to Nujira for more guidance in this area.

[2] LVDS Envelope Reference Data Timing Diagram is shown in Figure 6

[3] Standard product is pre-programmed for 122.88 Msps. Contact Nujira for information on variants

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

Output Characteristics							
Vout, L	Peak Output Power (Ppk)[4]	PAPR 6.5dB PAPR 8.5dB				500 650	W
	Average Output Power (Pavg)[5]					125	W
	Peak Output Current (Ipk)					10	A
	Vout Swing Range (Vout(max) – Vout(min))[6]				40	50	V
	Vout[7]			15		65	V
	Signal Bandwidth	WCDMA or LTE			20		MHz
	Tracking Accuracy	1Hz to 1MHz > 1MHz			0.2 0.2		V_{rms}
	Power Conversion Efficiency[8] (h) = Po(avg)/Σ (Main and Aux DC input powers)	WCDMA PAPR = 6.5dB			82		%
	Bulk Delay through coolteq.h modulator	Envelope signal input to Vout			4.8	4.9	µs
	SOA shutdown speed					100	ms

Test Methodology

The electrical characteristics were recorded using the test configuration shown in Figure 3. Bias Inductor Output (L) connector is coupled to PA Drain Voltage Output (Vout) via a Coilcraft SER2013-472 4.7 µH Bias Inductor. Resistive Load (R_L) is Nujira part number NCT-T5002 6.5 Ohm high power load.

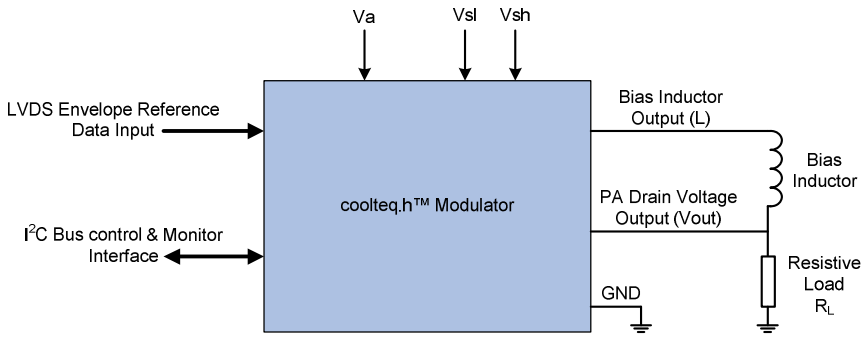


Figure 3: NCT-H4010 Test Configuration

[4] The Peak Output Power (Ppk) should not be exceeded in normal operation. Crest Factor Reduction modulation pre-processing should be used to limit the peak envelope excursion.
[5] The average output power is dependent on the Complementary Cumulative Distribution Function (CCDF) of the RF envelope. The maximum average output power is constrained by modulator thermal considerations.
[6] The typical voltage output range is 25 V to 65 V but is configurable subject to certain constraints; refer to Nujira for details.
[7] Subject to peak power conditions.
[8] Efficiency depends on usage configuration; refer to Nujira for details.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

8 Detailed Description

8.1 General Description

The coolteq.h® Modulator enables design of ultra high efficiency high crest factor RF power amplifiers with support for a wide range of PAPRs. The coolteq.h modulator design is RF frequency agnostic and operates in 20 MHz RF Bandwidth.

Figure 4 provides a conceptual model of the internal functionality of the coolteq.h modulator. The input LVDS envelope signal is passed through a 2 X interpolation filter before being fed into a DAC. Although there are other contributing blocks, the frequency response of the coolteq.h modulator is largely determined by this interpolation filter.

The output of the DAC is passed through a reconstruction filter creating the analogue reference signal for the output section of the modulator; this output block can be conceptualised as a high power, high bandwidth and high efficiency operational amplifier.

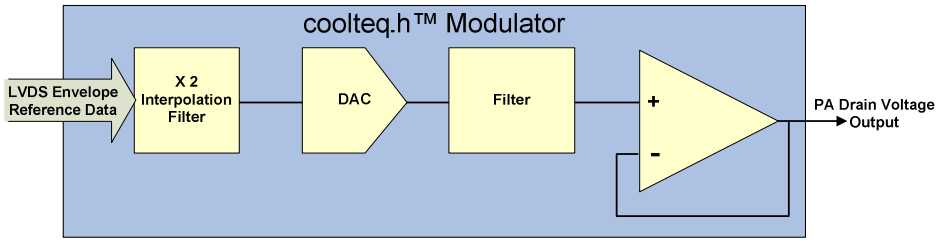


Figure 4: Model of coolteq.h modulator functionality

8.2 ET Amplifier System Overview

Figure 5 shows the block diagram of a digital envelope tracking amplifier. When implementing an envelope tracking digital amplifier the following additional aspects have to be considered compared to conventional fixed drain systems:

- Envelope Reference Data has to be created for the coolteq.h modulator (shaping) from the CFR-conditioned signal
- Implementation of control functionality for the coolteq.h modulator (Control & Monitor Interface)
- The delay between the RF signal and the Envelope Reference Data has to be controlled

Figure 5 shows the major blocks of the envelope tracking digital amplifier.

Both the lower pre-distortion (DPD) signal path and the upper envelope reference signal path are fed from a common CFR-conditioned input signal.

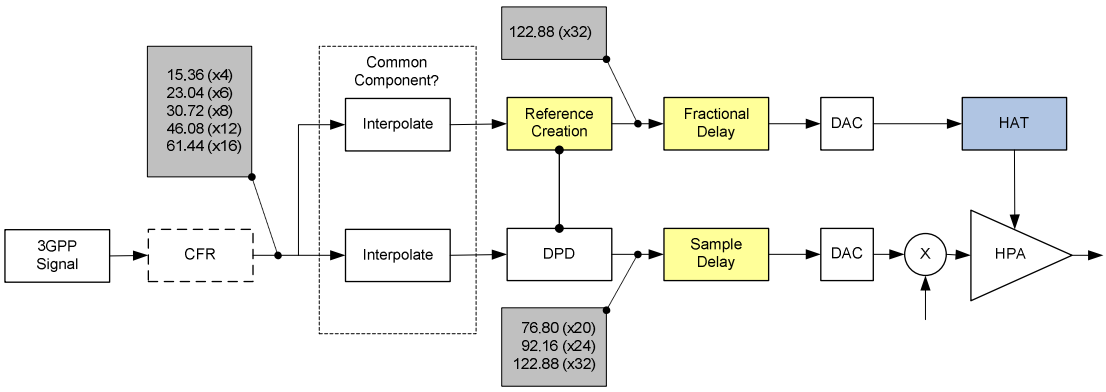


Figure 5: Block Diagram of Digital Envelope Tracking Amplifier

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

The coolteq.h modulator is designed to accept a reference input of 122.88 Msps which supports up to 50 MHz of signal bandwidth (wanted carriers plus pre-distortion). For 3GPP systems this signal input is typically generated from a composite multi-carrier signal of either 30.72 Msps or 61.44 Msps by a cascade of half band filters.

DPD solutions supporting 3 or more WCDMA carriers are typically found to operate with an input signal of 30.72, 46.08 or 61.44 Msps and produce an output sample rate of 92.16 or 122.88Msps. The 122.88 Msps reference rate for the modulator may therefore be derived using a 4x, 8/3x, or 2x interpolation filter and, in the case of integer multiples, the interpolation filtering may be shared.

8.3 Safe Operating Area

The coolteq.h modulator incorporates a Safe Operating Area protection mechanism that initiates a shut down when overload condition is detected. For information on how to identify an SOA event and how to restart the coolteq.h modulator please refer to [1].

In the case of a major instantaneous overload, the coolteq.h modulator shuts down and attempts to restart until the cause of the overload is resolved.

Output power is continually monitored to identify when a gradual increase in output power is likely to cause damage to the modulator. When the pre-damage threshold is reached the coolteq.h modulator shuts down and attempts to restart until the cause of the overload is resolved.

8.4 Envelope Reference Data Interface Bus

The LVDS Envelope Reference Data interface is a 14-bit parallel data-plus-clock interface providing the supply envelope waveform reference for the coolteq.h modulator.

The LVDS_CLK input forms the primary clock reference for analogue data conversion. This clock must be supplied from a low jitter source; therefore it should not be supplied via an FPGA.

The bus timing diagram is shown in Figure 6 (the electrical and timing characteristics are detailed in section 7).

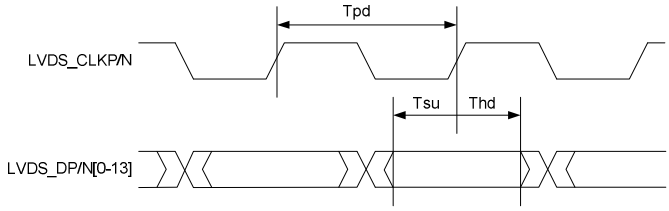


Figure 6: LVDS Envelope Reference Data Timing Diagram.

Mechanical details for the 50 pin Envelope, Control & Monitor Interface Connector are given in section 9.4. The LVDS inputs are terminated internally to the coolteq.h HAT modulator.

8.5 Control and Monitoring Interface

A typical coolteq.h modulator Control & Monitor Interface connection diagram is given in the Figure 7. In the figure, the Host monitors the alarm and warning status of the coolteq.h modulator via nHostInt interrupt line, and interacts with the coolteq.h modulator using the coolteq.h modulator Control & Monitor Interface Protocol through the I^2C connection. Utilisation of the nHostInt line is dependent upon the system design. The Host might use a polling-based control scheme in which nHostInt line might be polled.

The nResetIn line is utilised to reset the coolteq.h modulator by the Host without power cycling. The nResetOut becomes active when coolteq.h modulator is in reset state. Utilisation of the nResetOut line

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

is dependent upon the system design. The Host might poll the nResetOut line to detect if the coolteq.h modulator is reset due to a fault detection.

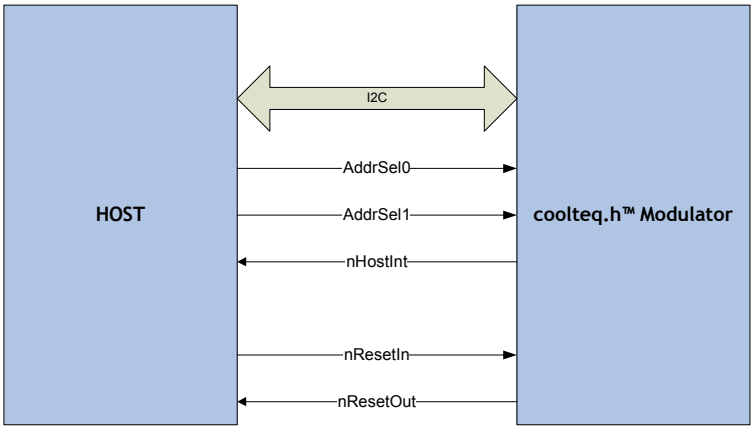


Figure 7: coolteq.h Modulator Control & Monitor Interface

8.5.1 I^2C Control & Monitor Bus

The I^2C bus is a standard Philips (now NXP) two wire serial interface, used for control and configuration of the coolteq.h modulator. This interface is not intended for real time data exchange. For further details, please refer to ref. [2]

The I^2C Control and Monitoring interface is used to manage the coolteq.h modulator through register reads and writes. It acts as a slave device and conforms to the Fast mode transfers. These registers make the following functions available to the host system:

- Modulator start-up
- Modulator shut-down
- Modulator reset
- Report product ID and serial number
- Report modulator status – temperature, warning & alarm states
- Reset modulator warning & alarm state
- Configure LVDS Envelope Reference Data Interface format
- Test LVDS data path
- Configure the user-programmable I^2C addresses
- Write and read operation parameters
- Download firmware
- Monitor the baseplate temperature
- Monitor the reset status

These functions are utilised using a protocol over I^2C bus based on a request & response scheme. Details of the protocol are given in [1]

This User Interface is not directly backwards-compatible with previous modulator interfaces

8.6 coolteq.h Modulator Operating Modes

The HAT modulator runs in one of the two operating modes; Modulation Mode and Maintenance Mode. The native operating mode of the HAT modulator is Modulation Mode. Therefore, the HAT modulator starts working in Modulation Mode after a reset or a power-on.
The HAT modulator can only switch to Maintenance Mode if the Host sends an *EnterMaintenanceMode* command. The HAT modulator switches back to Modulation Mode if the Host sends an *ExitMaintenanceMode* command.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

1. **Modulation Mode**: The HAT modulator's normal operational mode in which:

   - The HAT modulator can communicate with the Host
   - The HAT modulator always returns to Modulation Mode automatically after a reset
   - Configuration parameters cannot be changed
   - Software/Firmware cannot be downloaded into the HAT modulator
   - The HAT modulator can switch from one configuration set to another as a result of a Host request
   - Depending on the configuration, PA Drain Voltage Modulation is started automatically if there is no alarm (fault) condition.

2. **Maintenance Mode**: The HAT modulator's non-operational mode in which :

   - The HAT modulator can communicate with the Host
   - Configuration parameters and configuration sets can be manipulated
   - Software/Firmware can be downloaded into the HAT modulator in Maintenance Mode

   Note that the HAT modulator cannot provide PA drain voltage modulation in Maintenance Mode.

9 Application Information

9.1 Connection to RF Power Transistor

The connection between the Vout of the coolteq.h modulator and the drain of the RF Power Amplifier Transistor (PA) is critical to the performance of an Envelope Tracking PA. The coolteq.h modulator should be located as close to the 'cold' end of the PA drain bias feed line as is reasonably possible. RF decoupling should be performed using high quality RF capacitors of minimum value necessary for effective RF decoupling (approx. self resonant at RF operating frequency); refer to Nujira application note AN002077.

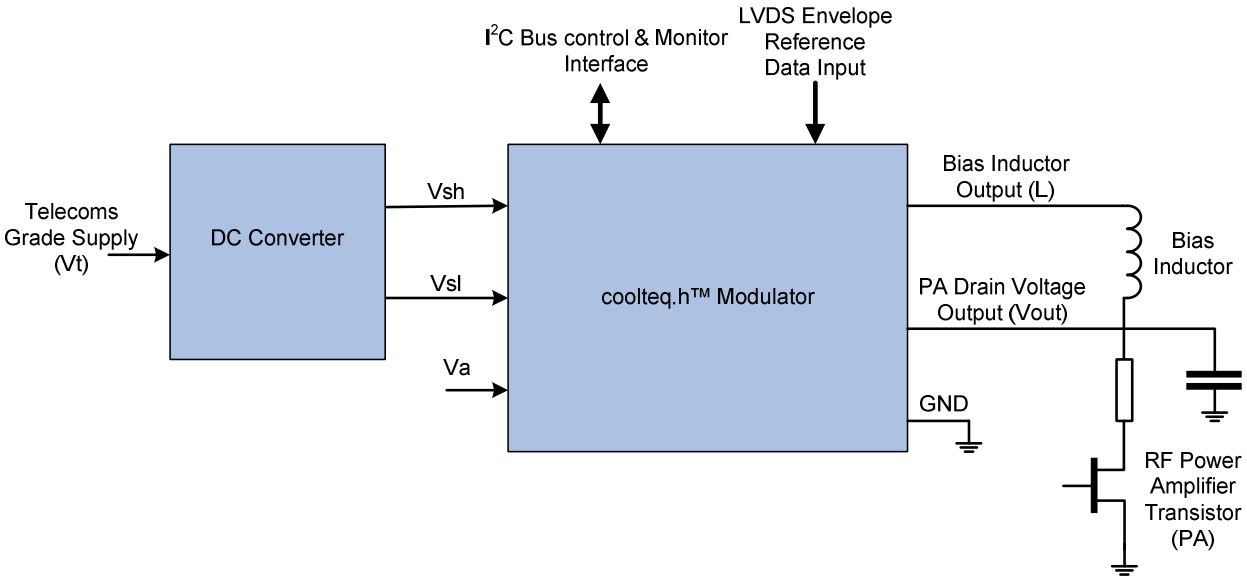


Figure 8 - Example PA application

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

9.2 RF Power Amplifier Transistor Matching

The efficiency of the combined RF Power Amplifier Transistor and coolteq.h modulator is influenced by the source and load impedance of the RF Power Amplifier Transistor. The optimum match for an ET amplifier is not the same as that for a conventional fixed drain amplifier, as the ET amplifier average drain voltage is substantially less than that of a fixed drain amplifier. In addition to ensuring that the RF Power Amplifier Transistor's RF load impedance is correct it is also important that the RF Power Amplifier Transistor presents the correct impedance to the coolteq.h modulator at "video" frequencies (up to 200 MHz). Please contact Nujira for further details.

9.3 Thermal and Mechanical Considerations

Thermal relief of the coolteq.h modulator is accomplished by mounting the modulator directly onto the top surface of the RF Pallet heat sink through a cut-out in the RF Pallet PCB and secured using machine screws to ensure good thermal contact. The critical PA Drain Voltage Output (Vout) connection between the coolteq.h modulator and the RF Power Amplifier Transistor drain is made using low inductance output tabs (signal and ground). DC power supplies to the modulator are made through an ERNI MicroPower connector. The Envelope, Control & Monitor Interface signals are provided through a multi-way IDC connector mounted at one end of the coolteq.h modulator.

The coolteq.h modulator Envelope, Control & Monitor Connector emerges horizontally from the coolteq.h modulator to mate with a cable connector, part number: ERNI 024403. The Input Supply Connector on the underside of the coolteq.h modulator mates with an ERNI MicroSpeed Power connector, part number: ERNI 214547. The vertical positioning of the coolteq.h modulator must be such that the gap between the power connectors does not exceed 1mm, and that the PA Drain voltage output tabs sit flat on to the RF PA pallet. Please consult Nujira for information on connector height.

9.4 Connectors

9.4.1 50-Pin Connector Details

The Envelope, Control & Monitor Interface connector on the coolteq.h modulators has 50 signal pins as listed in Section 5

The coolteq.h modulator Envelope, Control & Monitor connector emerges horizontally from the coolteq.h modulator to mate with a cable connector, part number: ERNI 024403. Reference pin location (Pin 1) on the connector is given in Figure 9.

Figure 9: Pin locations of LVDS Envelope, Control & Monitor connector

The coolteq.h modulator Envelope, Control & Monitor connector is a 50 pin, 1.27mm pitch male surface mounted connector from ERNI, part number: 154765, mechanical details as shown in Figure 10.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

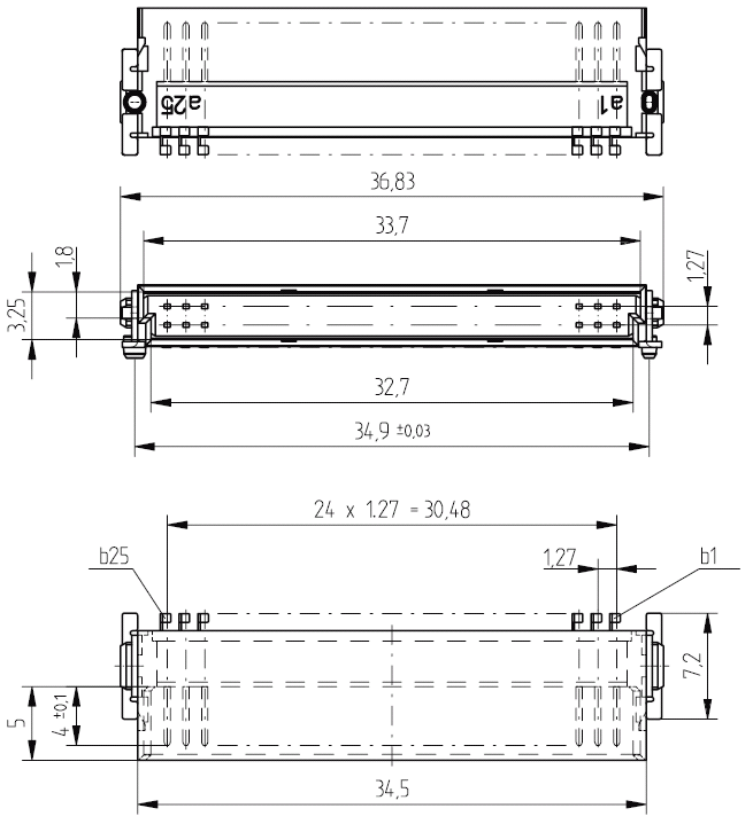


Figure 10: 50-Pin Connector Mechanical Drawings

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

9.4.2 Envelope, Control & Monitor Interface, Ribbon Cable Connector Details

The coolteq.h modulator Envelope, Control & Monitor Interface connector is designed to mate with a 50 pin female ribbon cable IDC connector from ERNI, part number: 024403. The mechanical drawing of the ribbon cable connector is given in Figure 11.

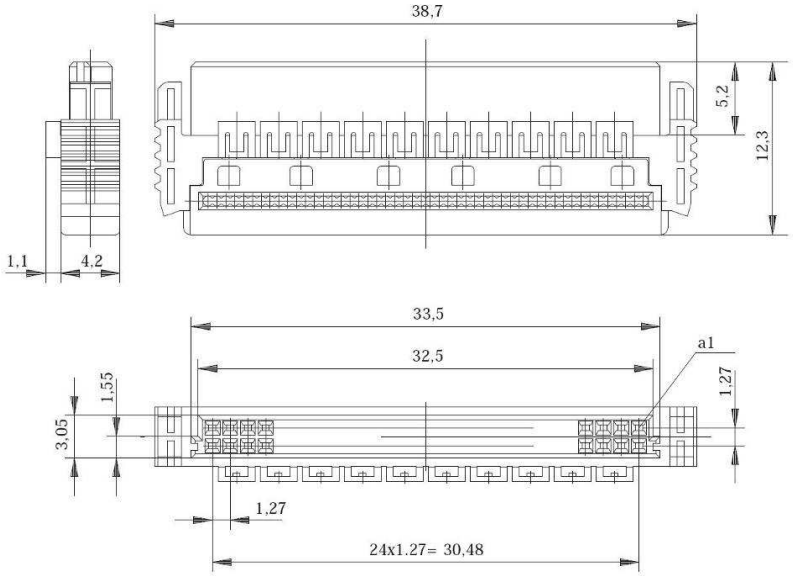


Figure 11: coolteq.h Modulator Envelope, Control & Monitor Interface, Ribbon Cable Connector Mechanical Drawings

9.4.3 Envelope, Control & Monitor Interface, Ribbon Cable Specifications

The female ribbon cable IDC connector is designed to be crimped onto 0.635mm pitch ribbon cable, and the length of this ribbon cable should be less than 300mm. The ribbon cable should fulfil the specifications given in Table 1.

Wire size	:	AWG30, stranded, tin plated
Wire stranding	:	7 * 0.102 (7/38“)
Insulation	:	PVC, flame retardant VW-1, red stripe
Conductor spacing	:	0.635 mm (0.025“)
Temperature range	:	-20°C... + 105°C
Voltage rating	:	150V
Test voltage	:	1500Veff
Conductor resistance	:	max. 354Ω/km
Capacitance at 1 kHz	:	95 pF/m
Inductance at 10 kHz	:	0.5µH/m
Insulation resistance	:	min. 30MΩ x km
UL-Style	:	E2678

Table 1: Envelope, Control & Monitor Interface, Ribbon Cable Specifications

9.4.4 Envelope, Control & Monitor Interface Connector Termination

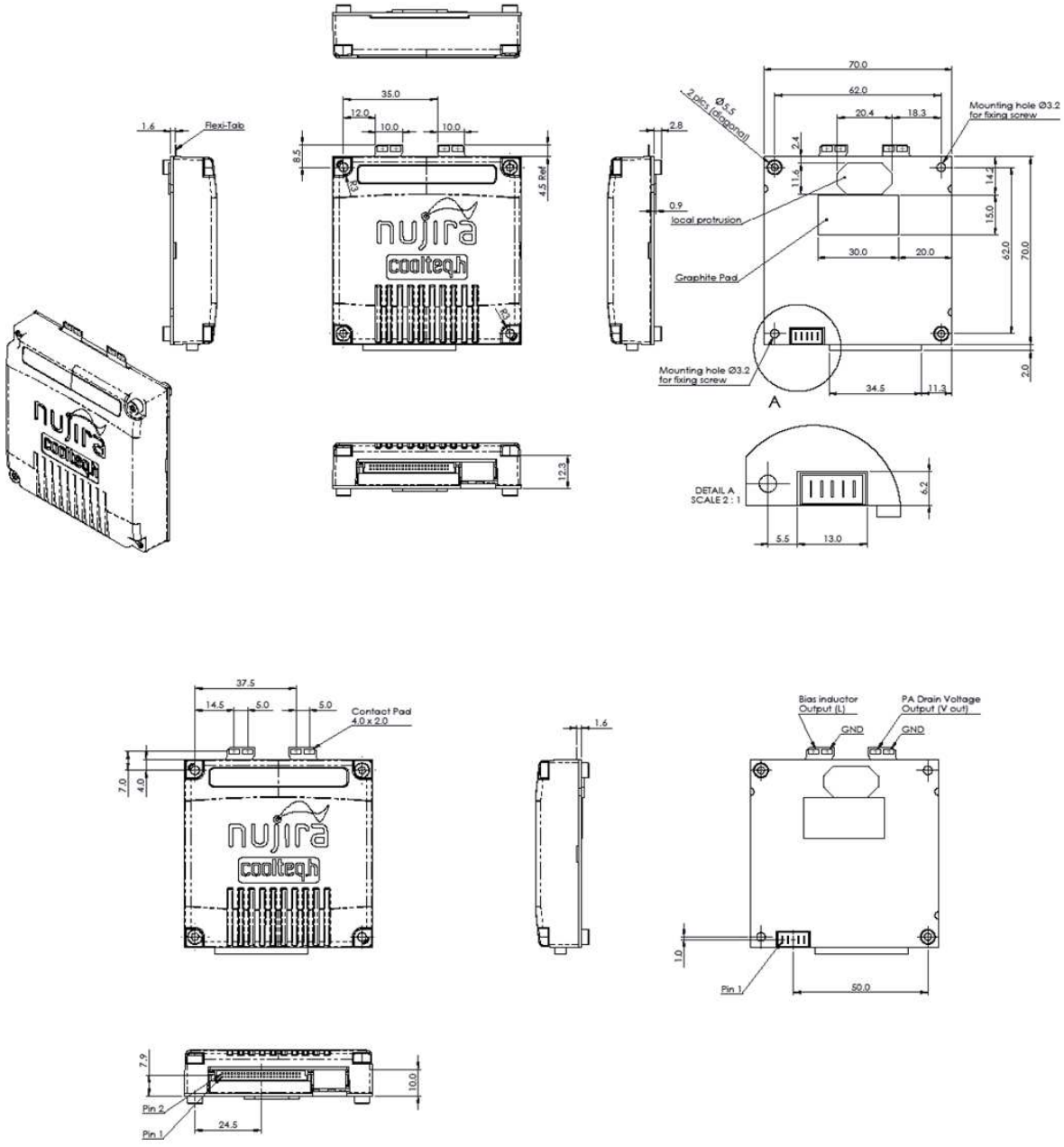
The LVCMOS inputs are 5 V tolerant. For the Open Drain (OD) outputs, use a 4.7 kΩ or greater pull-up resistor. These outputs are 5 V tolerant. The LVDS inputs are terminated internally to the coolteq.h HAT modulator.
Please refer to the I^2C specification [2] for the termination of I^2C pins.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

10 Package details

Base mechanical drawing HMP-6: DA100700.2.0.DD1



PARAMETER	TYP	UNIT
Weight	210	g

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

11 Regulatory Specifications

PARAMETER	REFERENCE
The modulator is compliant with the following standards:	
Storage	ETSI EN 300 019-1-1 Class 1.2 weather-protected
Transportation	ETSI EN 300 019-1-2 Class 2.3 public
Operation	ETSI EN 300 019-1-4 Class 4.1 non-weather-protected
Shock & Vibration	ETSI EN 300 019-2-4 Class 4.1 non-weather-protected
Safety	IEC/UL 60950
The modulator is designed (and tested where and as appropriate) to enable the host product to be compliant with the appropriate parts of the following standards:	
R & TTE	ETSI EN 301 489
EMC	FCC Part 15 sub-part B, EN55022, EN55024
Base Station Performance	ANSI/TIA/EIA-97-D

Note: EMC performance is dependent on system design as described in application note AN002077 [5].

Abbreviations

ABBREVIATION	MEANING
CFR	Crest Factor Reduction
DAC	Digital to Analogue Converter
DPD	Digital Pre-Distortion
EMC	Electro-magnetic compatibility
HAT®	High Accuracy Tracking
HPA	High Power Amplifier
IDC	Insulation Displacement Connector
OD	Open Drain
PAPR	Peak to Average Power Ratio
SOA	Safe Operating Area

References

[1] Version 3 Control and Monitoring Interface, PD002239, Nujira Ltd.

[2] The I^2C-Bus Specification, version 2.1, January 2000, 9398 393 40011, Philips (now NXP)

[3] Nujira Baseband Interface Specification V2.1, PD002091, Nujira Ltd.

[4] User Guide V3.1, AN002098, Nujira Ltd.

[5] Design Guide V1.5, AN002077, Nujira Ltd.

Copyright © Nujira Ltd. 2011

UNCLASSIFIED

Contact Information

Nujira Limited
Building 1010
Cambourne Business Park
Cambourne, Cambridge
CB23 6DP
United Kingdom

Tel: +44 (0) 1223 597900
Fax: +44 (0) 1223 597972

Email: info@nujira.com
Internet: www.nujira.com

COPYRIGHT © NUJIRA LIMITED 2011. ALL RIGHTS RESERVED.

REPRODUCTION, TRANSFER OR DISTRIBUTION OF THIS DOCUMENT IN ANY FORM WITHOUT THE PRIOR WRITTEN PERMISSION OF NUJIRA LIMITED IS PROHIBITED.

NUJIRA LIMITED AND/OR ITS RESPECTIVE SUPPLIERS MAKE NO REPRESENTATIONS ABOUT THE SUITABILITY OF THE INFORMATION CONTAINED IN THIS DOCUMENT FOR ANY PURPOSE. THIS DOCUMENT IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND. NUJIRA LTD AND/OR ITS RESPECTIVE SUPPLIERS HEREBY DISCLAIM ALL WARRANTIES AND CONDITIONS WITH REGARD TO THIS INFORMATION, INCLUDING ALL IMPLIED WARRANTIES AND CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE AND NON-INFRINGEMENT. IN NO EVENT SHALL NUJIRA LTD AND/OR ITS RESPECTIVE SUPPLIERS BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF INFORMATION AVAILABLE FROM THIS DOCUMENT.

THE DOCUMENT COULD INCLUDE TECHNICAL INACCURACIES OR TYPOGRAPHICAL ERRORS. CHANGES ARE PERIODICALLY ADDED TO THE INFORMATION HEREIN. NUJIRA LTD AND/OR ITS RESPECTIVE SUPPLIERS MAY MAKE IMPROVEMENTS AND/OR CHANGES IN THE PRODUCT(S) AND/OR THE PROGRAM(S) DESCRIBED HEREIN AT ANY TIME.

You have no obligation to give Nujira any suggestions, comments or other feedback ("Feedback") relating to this Specification.

However, any Feedback you voluntarily provide may be used in Nujira products and related specifications or other documentation which in turn may be relied upon by other third parties to develop their own products. Accordingly, if you do give Nujira Feedback on any version of this Specification you agree that: (a) Nujira may freely use, reproduce, license, distribute, and otherwise commercialize your Feedback; (b) you also grant third parties, without charge, only those patent rights necessary to enable other products to use or interface with any specific parts of a Nujira product that incorporate your Feedback; and (c) you will not give Nujira any Feedback (i) that you have reason to believe is subject to any patent, copyright or other intellectual property claim or right of any third party; or (ii) is subject to license terms which seek to require any Nujira product incorporating or derived from such Feedback, or other Nujira intellectual property, to be licensed to or otherwise shared with any third party.