coolteq.h Modulator Baseband Interface

PD002091

1 Introduction

This Application Note provides a description of the physical interface for a baseband system to connect to the Envelope, Control & Monitor Interface of Nujira coolteq.h™ NCT-H30xx and NCT40xx Modulators.

2 Connector Pin Assignment

The Envelope, Control & Monitor Interface connector on the coolteq.h™ Modulators has 50 signal pins as listed in the **Table 1**.

Dir.	Type	Name	Pin No		Name	Type	Dir.
I	LVCMOS	AddrSel0	1	2	GND	-	-
I	LVCMOS	AddrSel1	3	4	I2C_SCL	I2C	I / OD
I	LVCMOS	TDDPowerSave	5	6	I2C_SDA	I2C	I / OD
O	OD	nHostInt	7	8	GND	-	-
-	-	GND	9	10	GND	-	-
I	LVDS	LVDS_CLKP	11	12	LVDS_CLKN	LVDS	I
-	-	GND	13	14	GND	-	-
I	LVDS	LVDS_DP0	15	16	LVDS_DN0	LVDS	I
I	LVDS	LVDS_DP1	17	18	LVDS_DN1	LVDS	I
I	LVDS	LVDS_DP2	19	20	LVDS_DN2	LVDS	I
I	LVDS	LVDS_DP3	21	22	LVDS_DN3	LVDS	I
I	LVDS	LVDS_DP4	23	24	LVDS_DN4	LVDS	I
-	-	GND	25	26	GND	-	-
I	LVDS	LVDS_DP5	27	28	LVDS_DN5	LVDS	I
I	LVDS	LVDS_DP6	29	30	LVDS_DN6	LVDS	I
-	-	GND	31	32	GND	-	-
I	LVDS	LVDS_DP7	33	34	LVDS_DN7	LVDS	I
I	LVDS	LVDS_DP8	35	36	LVDS_DN8	LVDS	I
-	-	GND	37	38	GND	-	-
I	LVDS	LVDS_DP9	39	40	LVDS_DN9	LVDS	I
I	LVDS	LVDS_DP10	41	42	LVDS_DN10	LVDS	I
I	LVDS	LVDS_DP11	43	44	LVDS_DN11	LVDS	I
I	LVDS	LVDS_DP12	45	46	LVDS_DN12	LVDS	I
I	LVDS	LVDS_DP13	47	48	LVDS_DN13	LVDS	I
O	OD	nResetOut	49	50	nResetIn	LVCMOS	I

I:Input, O:Output, OD:Open Drain

Table 1. coolteq.h™ Modulator, Envelope, Control & Monitor Interface connector.

The coolteq.h™ Modulator Envelope, Control & Monitor connector emerges horizontally from the coolteq.h™ Modulator to mate with a cable connector, part number: ERNI 024403. Reference pin location (Pin 1) on the connector is given in the **Figure 1**.

Figure 1. Reference pin location of LVDS Envelope, Control & Monitor connector.

3 Electrical Characteristics

Electrical characteristics of coolteq.h™ Modulator Envelope, Control & Monitor Interface are given in this section.

3.1 Signal Name Definitions

coolteq.h™ Modulator Envelope, Control & Monitor Interface electrical signal name definitions are given in **Table 2**.

Signal Name	Definition
GND	Ground
AddrSel0, AddrSel1	I^2C address setting
I2C_SCL	I^2C Serial Clock
I2C_SDA	I^2C Serial Data
TDDPowerSave	User programmable TDD Mode Power Saving signalling input. If this pin is not utilised, it should be connected to Ground. For programming details please refer to [3]
nHostInt	User Programmable Alarm and Warning status signal, active LOW. For programming details please refer to [3]
nResetIn	coolteq.h™ Modulator reset input, active LOW. If this signal is not utilised, it should be left unconnected.
nResetOut	coolteq.h™ Modulator reset indicator output, active LOW
LVDS_CLKP, LVDS_CLKN	LVDS Data Clock Lines
LVDS_DP0-13, LVDS_DN0-13	LVDS Data Bus Lines x14

Table 2. Signal Name Definitions.

The LVDS_CLK input forms the primary clock reference for analogue data conversion. This clock must be supplied from a low jitter source; therefore it is not suitable to be supplied via an FPGA.

3.2 Electrical Levels

Electrical signal levels are given in **Table 3**.

Type	Parameter		Min	Typ	Max
LVDS	V_{CM},	Voltage Common Mode	$(\|V_{ID}\|/2)V$	-	$(2.4-\|V_{ID}\|/2)V$
	$V_{ID,}$	Voltage Input Differential	0.1V	-	0.6V
LVCMOS	V_{IL},	Input Low Voltage	0.0V	-	0.8V
	V_{IH},	Input High Voltage	2.2V	-	3.3V
OD	V_{OCOL},	OC Output Low Voltage	-	-	0.6V

Table 3. Electrical Signal Levels.

The LVCMOS inputs are 5V tolerant. For the Open Drain (OD) outputs use a 4.7K or greater pull-up resistor. These outputs are 5V tolerant.
The LVDS inputs are terminated internally to the coolteq.hHAT™ Modulator.
On how to interface to the I2C pins please refer to the I2C specification [4].

3.3 LVDS Envelope Reference Data Interface Bus Timing

The LVDS Envelope Reference Data interface is a 14 parallel data plus clock interface providing the supply envelope reference data for the coolteq.h™ Modulator through Envelope, Control & Monitor Interface Connector. The bus timing diagram is given in **Figure 2**.

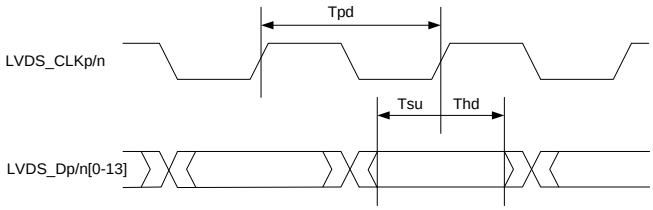

Figure 2. LVDS Envelope Reference Data Timing Diagram.

Timing parameters are given in the **Table 4**.

Parameter	Description	Min	Typ	Max
Tpd	LVDS_CLKp/n Clock Period	-	1/122.88µs	-
Tsu	LVDS_Dp/n[0-13] Stable to LVDS_CLKp/n Low (Setup)	3ns	-	-
Thd	LVDS_CLKp/n Low to LVDS_Dp/n[0-13] Change (Hold)	2ns	-	-

Table 4. LVDS Envelope Reference Bus Timing.

3.4 I²C Bus Timing

The I²C bus is a standard Philips two wire serial interface for control and configuration of the coolteq.h™ Modulator. This interface is not intended for real time data exchange. For further details, please refer to [4].

4 Mechanical Details

4.1 Envelope, Control & Monitor Interface, Connector Details

The coolteq.h™ Modulator Envelope, Control & Monitor connector is a 50 pin, 1.27mm pitch male surface mounted connector from ERNI, part number: 154765.

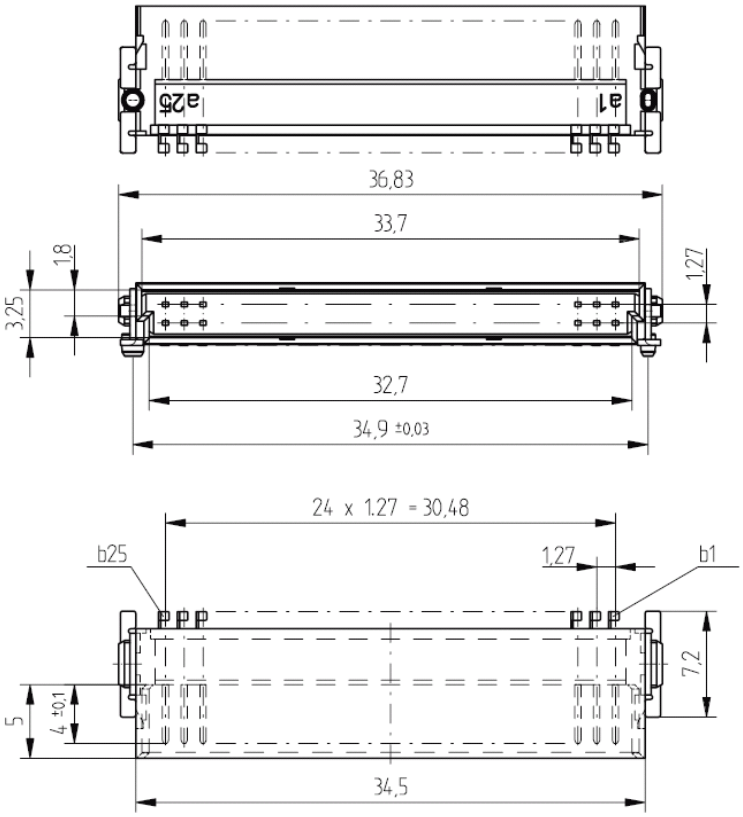

Figure 3. coolteq.h™ Modulator Envelope, Control & Monitor Interface, Connector Mechanical Drawings.

4.2 Envelope, Control & Monitor Interface, Ribbon Cable Connector Details

The coolteq.h™ Modulator Envelope, Control & Monitor Interface connector is designed to mate with a 50 pin female ribbon cable IDC connector from ERNI, part number: 024403. The mechanical drawing of the ribbon cable connector is given in **Figure 4**.

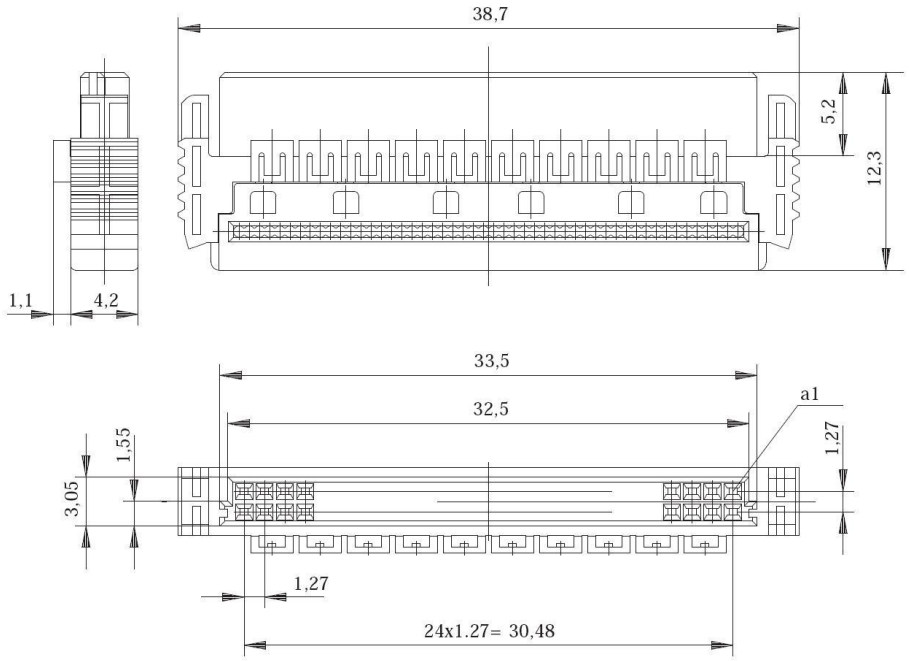

Figure 4. coolteq.h™ Modulator Envelope, Control & Monitor Interface, Ribbon Cable Connector Mechanical Drawings.

4.3 Envelope, Control & Monitor Interface, Ribbon Cable Specifications

The female ribbon cable IDC (Insulation Displacement Connector) connector is designed to be crimped onto 0.635mm pitch ribbon cable, and the length of this ribbon cable should be less than 1 meter. The ribbon cable should fulfil the specifications given in **Table 5**.

Wire size	:	AWG30, stranded, tin plated
Wire stranding	:	7 * 0.102 (7/38“)
Insulation	:	PVC, flame retardant VW-1, red stripe
Conductor spacing	:	0.635 mm (0.025“)
Temperature range	:	-20°C... + 105°C
Voltage rating	:	150V
Test voltage	:	1500Veff
Conductor resistance	:	max. 354Ω/km
Capacitance at 1 kHz	:	95 pF/m
Inductance at 10 kHz	:	0.5µH/m
Insulation resistance	:	min. 30MΩ x km
UL-Style	:	E2678

Table 5. Envelope, Control & Monitor Interface, Ribbon Cable Specifications

5 References

[1] coolteq.h™ Modulator Design Guide, Nujira Ltd. AN002077.

[2] coolteq.h™ NCT-H3010 / NCT-H4010 Modulator Preliminary Datasheets, Nujira Ltd.

[3] coolteq.h™ Version 3 Control Interface Specification, Nujira Ltd. PD002239.

[4] The I^2C Specification, version 2.1, January 2001, Philips Doc No 9398 393 40011.

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